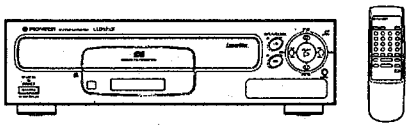
PIONEER®
The Art of Entertainment

Service Manual



ORDER NO.
RRV1342

CD CDV LD PLAYER

CLD-S310
CLD-S310F
CLD-S310S

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Type	Model			Power Requirement	Remarks
	CLD-S310	CLD-S310F	CLD-S310S		
WBW	○	–	–	AC220-240V	
WEZ	○	–	–	AC220-240V	
WEZW/FR	–	○	–	AC220-240V	
WEZW/SP	–	–	○	AC220-240V	

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1. SAFETY INFORMATION

(FOR EUROPEAN MODEL ONLY)

VARO!
AVATTAESSA JA SUOJALUKITUS OHITETTAESSA OLET ALTTIINA NÄKYMÄTTÖMÄLLE LASERSÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN.

ADVERSEL:
USYNLIG LASERSTRÅLING VED ÅBNING NÅR SIKKERHEDSAFBRYDERE ER UDE AF FUNKTION UNDGÅ UDSAETTELSE FOR STRÅLING.

VARNING!
OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD OCH SPÄRREN ÄR URKOPPLAD. BETRAKTA EJ STRÅLEN.

LASER
Kuva 1
Lasersateilyn
varoitusmerkki

WARNING!
DEVICE INCLUDES LASER DIODE WHICH EMITS INVISIBLE INFRARED RADIATION WHICH IS DANGEROUS TO EYES. THERE IS A WARNING SIGN ACCORDING TO PICTURE 1 INSIDE THE DEVICE CLOSE TO THE LASER DIODE.

IMPORTANT
THIS PIONEER APPARATUS CONTAINS LASER OF CLASS 1.
SERVICING OPERATION OF THE APPARATUS SHOULD BE DONE BY A SPECIALLY INSTRUCTED PERSON.

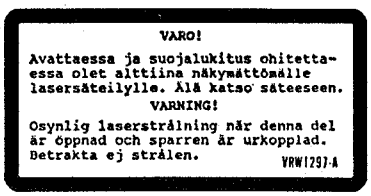
LASER DIODE CHARACTERISTICS
MAXIMUM OUTPUT POWER: 5 mw
WAVELENGTH: 780-785 nm

LASER
Picture 1
Warning sign for
laser radiation

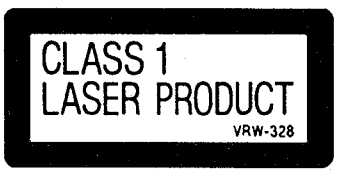
LABEL CHECK

WBW type

WEZ, WEZW/FR and WEZW/SP types

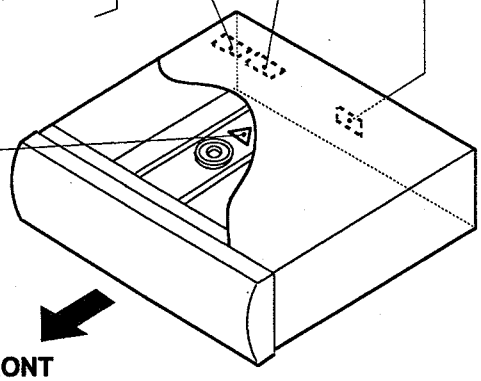


All types



WEZ, WEZW/FR and WEZW/SP types

All types



FRONT

Additional Laser Caution

1. The ON/OFF statuses of the slider-position detection switches (PARK INNER, PARK OUTER on the PKSB assy), loading-status detection switches (SW 1, 2 and 3 on LMSB assy) are detected by the microprocessor (IC101 in the MOTHER assy). To permit the laser diode to oscillate, it is required to set the slider-position detection switch for the LD ACTIVE status (PARK INNER : OFF, PARK OUTER : OFF), and to set the loading-status detection switch for tilt neutral state (SW1 : OFF, SW2 : OFF, SW3 : ON). As long as these requirements are not satisfied, the laser diode will not oscillate. When the requirements are met in any way, the laser diode can oscillate. The laser diode oscillation will continue if pin 13 of IC801 is shorted to GND or the emitter and collector of Q834 are shorted each other (fault condition) in MOTHER assy.
   In test mode ＊, the laser diode oscillates when microprocessor detects a PLAY signal, or when the PLAY key is pressed (S205 ON on the KEYB assy), with the above requirements satisfied.
2. When the cover is open, close viewing through the objective lens with the naked eye will cause exposure to a Class 1 laser beam.

＊ : Refer to page 34.

2. PACKING, EXPLODED VIEWS AND PARTS LIST

NOTES:
- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*
- *Parts list without notice are common for CLD-S310/WBW, WEZ, CLD-S310F/WEZW/FR and CLD-S310S/WEZW/SP.*

2.1 PACKING

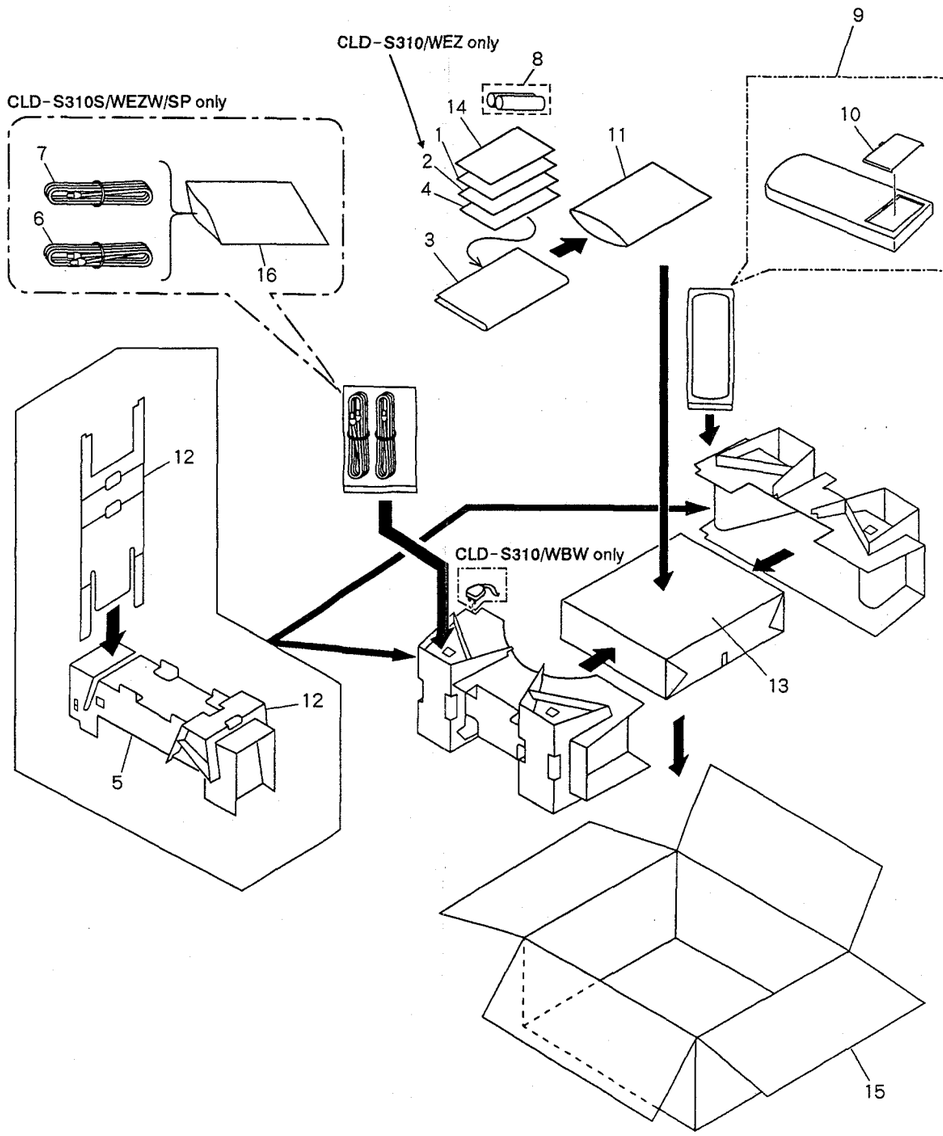
(1) CONTRAST OF CLD-S310/WBW, WEZ, CLD-S310F/WEZW/FR and CLD-S310S/WEZW/SP

CLD-S310/WBW, WEZ, CLD-S310F/WEZW/FR and CLD-S310S/WEZW/SP have the same construction except for the following:

Mark	No.	Symbol & Description	Part No.				Remarks
			CLD-S310 /WBW	CLD-S310 /WEZ	CLD-S310F /WEZW/FR	CLD-S310S /WEZW/SP	
NSP	1	Caution (UC)	VRR1020	Not used	Not used	Not used	
NSP	1	Caution (EW)	Not used	VRM1027	VRM1027	VRM1027	
NSP	2	Caution	Not used	VRR1009	Not used	Not used	
	3	Operating instructions (English/French/German/Italian)	VRE1034	VRE1034	Not used	Not used	
	4	Operating instructions (Dutch/Swedish/Spanish/Portuguese)	Not used	VRF1033	Not used	Not used	
	4	Operating instructions (French)	Not used	Not used	VRC1041	Not used	
	4	Operating instructions (Spanish)	Not used	Not used	Not used	VRC1042	
	6	Audio cord	Not used	Not used	Not used	VDE1033	
	7	Video cord	Not used	Not used	Not used	VDE1034	
	15	Packing case	VHG1446	VHG1446	VHG1450	VHG1451	
NSP	16	Polyethylene bag	Not used	Not used	Not used	Z21-038	

(2) PARTS LIST FOR CLD-S310/WBW

Mark	No.	Description	Part No.
	1	Caution (UC)	VRR1020
	2	•••••	
	3	Operating instructions (English/French/German/Italian)	VRE1034
	4	•••••	
	5	Protector	VHB1007
	6	•••••	
	7	•••••	
NSP	8	Battery (R6P, AA)	VEM-013
	9	Remote control unit	VXX2268
	10	Battery cover	VNK2806
NSP	11	Polyethylene bag	VHL-014
	12	Protector B	VHB1012
	13	Mirror mat sheet	Z23-007
NSP	14	Warranty card	ARW-088
	15	Packing case	VHG1446
	16	•••••	



2.2 EXTERIOR AND DISC TRAY SECTION

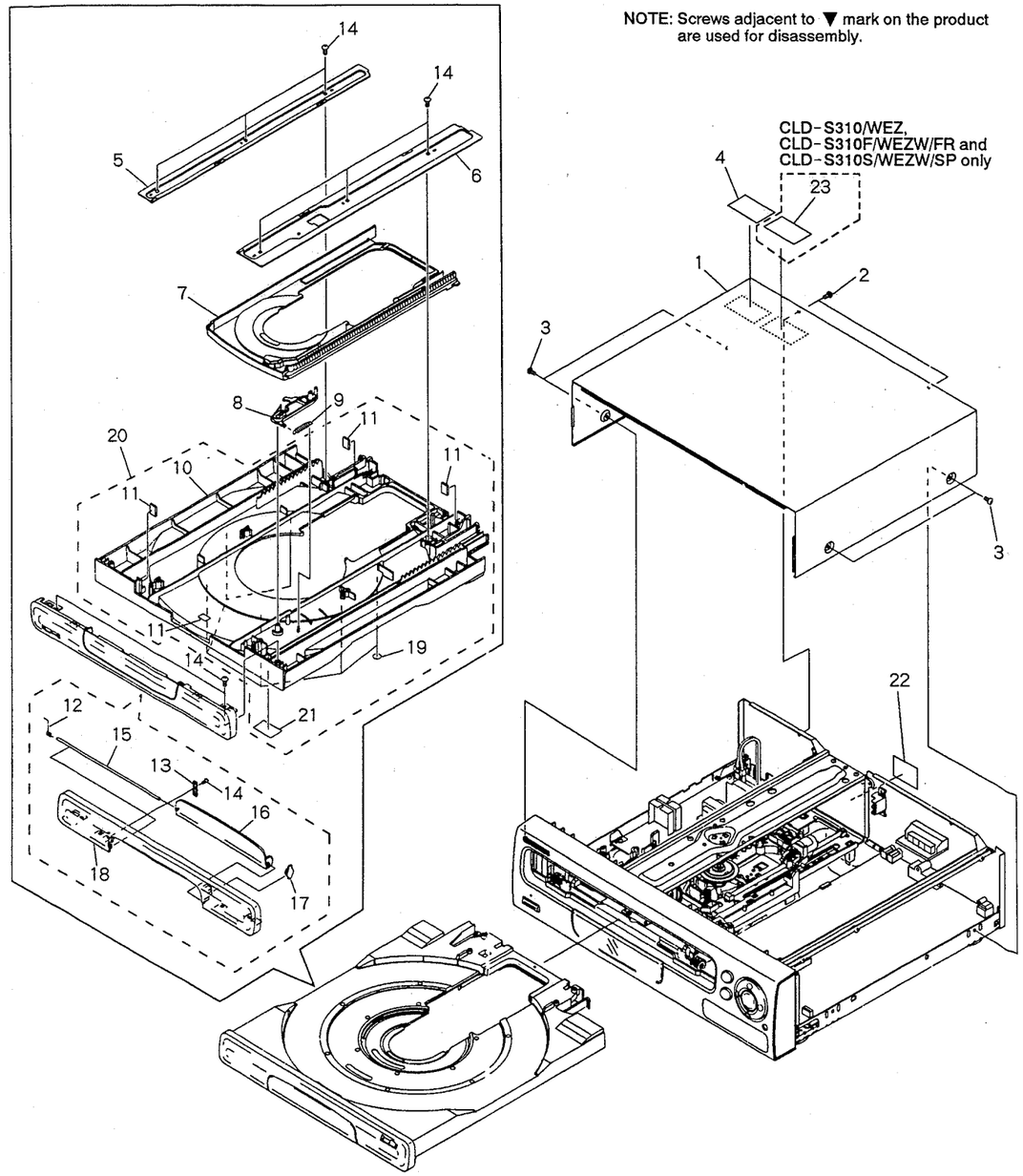
(1) CONTRAST OF CLD-S310/WBW, WEZ, CLD-S310F/WEZW/FR and CLD-S310S/WEZW/SP

CLD-S310/WBW, WEZ, CLD-S310F/WEZW/FR and CLD-S310S/WEZW/SP have the same construction except for the following:

Mark	No.	Symbol & Description	Part No.				Remarks
			CLD-S310 /WBW	CLD-S310 /WEZ	CLD-S310F /WEZW/FR	CLD-S310S /WEZW/SP	
	4	Caution label	PRW1018	VRW1094	VRW1094	VRW1094	
	23	Caution label HE	Not used	VRW1297	VRW1297	VRW1297	

(2) PARTS LIST FOR CLD-S310/WBW

Mark	No.	Description	Part No.
	1	Bonnet-S	VXX2117
	2	Screw	BBZ30P080FMC
	3	Screw	BCZ40P060FZK
	4	Caution label	PRW1018
	5	Guide plate (R)	VNE1939
	6	Guide plate (L)	VNE1938
	7	CD tray	VNK2687
	8	Lock plate	VNL1703
	9	Lock plate spring	VBH1188
NSP	10	LD tray	VNK2686
	11	Damp cushion	VEC1683
	12	Door spring	VBH1247
	13	Door holder	VNL1658
	14	Screw	BBZ30P080FMC
	15	Door shaft	VLL1455
	16	CD door	VNK2791
	17	Damper assy	VXA1999
	18	Tray panel	VNK2801
	19	Disc pad	VEC1682
	20	Tray assy-S	VXX2171
NSP	21	Label	VRW1289
NSP	22	Caution label (F)	VRW-328
	23	•••••	

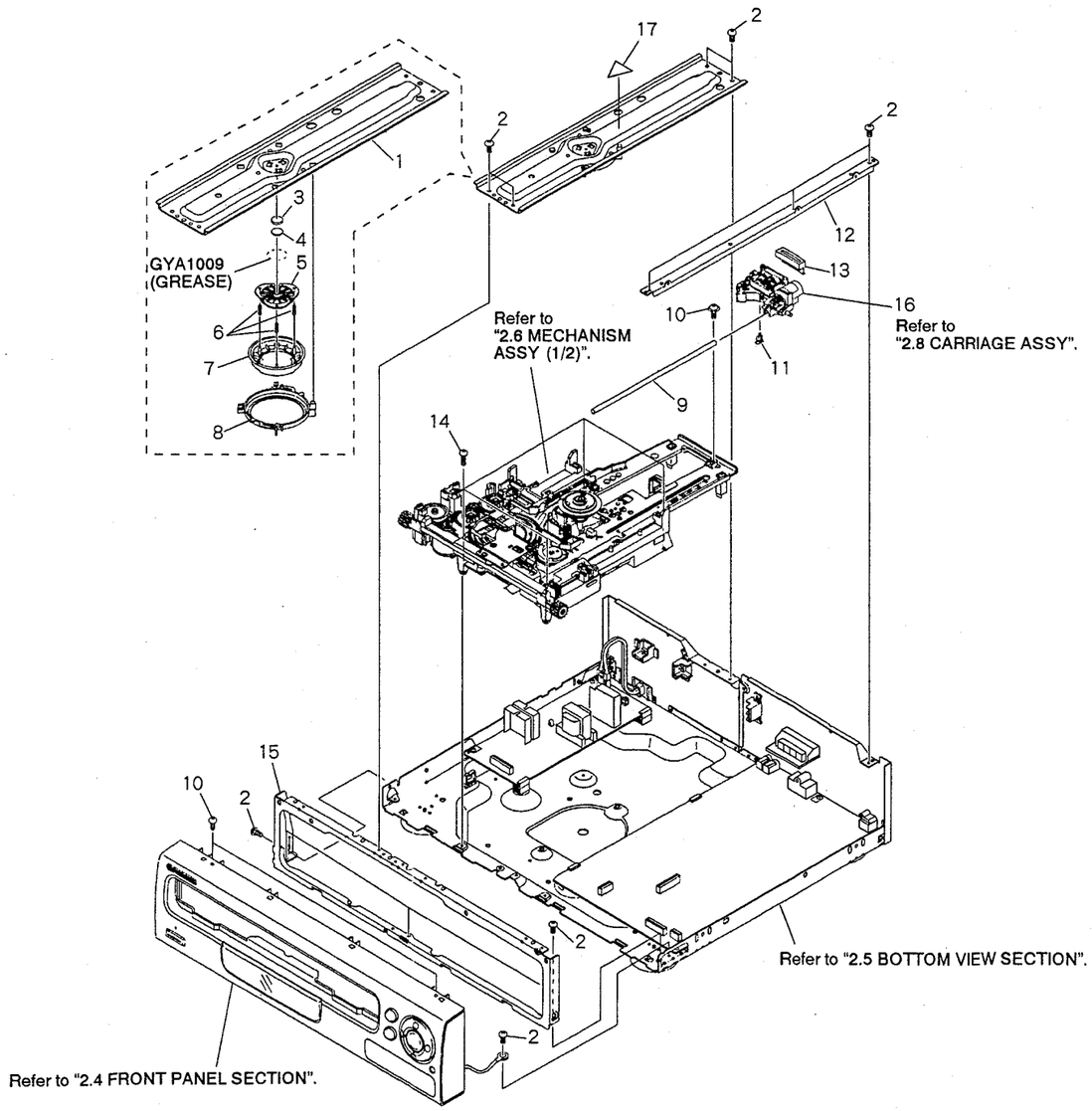


NOTE: Screws adjacent to ▼ mark on the product are used for disassembly.

2.3 TOP VIEW SECTION

Parts List

Mark	No.	Description	Part No.
	1	Clamper arm	VNE1940
	2	Screw	BBZ30P080FMC
	3	Rubber sheet	VEB1114
	4	Thrust holder	VNL1663
	5	Clamper head	VNL1649
	6	Clamp spring	VBH1192
	7	Clamper	VNL1648
	8	Clamper holder	VNL1636
	9	Guide bar	VLL1453
	10	Screw	IBZ30P080FMC
	11	CA hook	VNL1641
NSP	12	PCB holder	VNE2034
	13	FFC holder	VNL1656
	14	Screw	BBZ30P100FMC
NSP	15	Panel holder	VNA1464
	16	Carriage assy	VWT1110
	17	Caution label (G)	VRW-329



2.4 FRONT PANEL SECTION

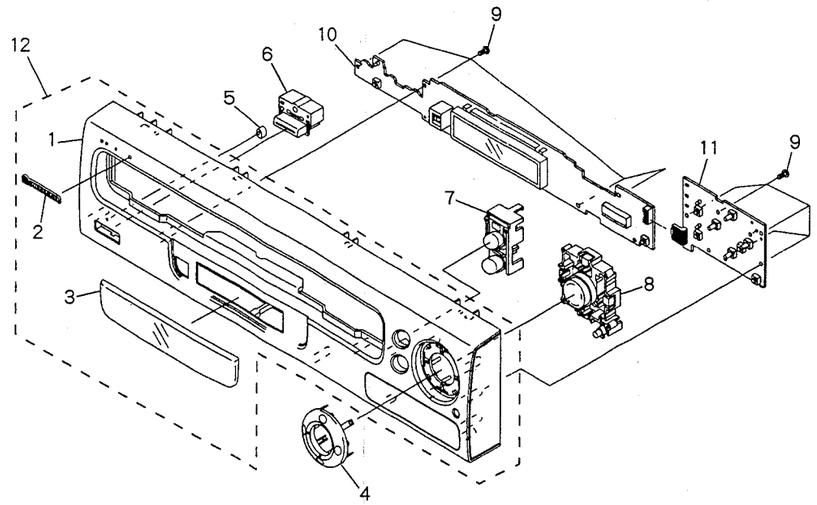
(1) CONTRAST OF CLD-S310/WBW, WEZ, CLD-S310F/WEZW/FR and CLD-S310S/WEZW/SP

CLD-S310/WBW, WEZ, CLD-S310F/WEZW/FR and CLD-S310S/WEZW/SP have the same construction except for the following:

Mark	No.	Symbol & Description	Part No.				Remarks
			CLD-S310 /WBW	CLD-S310 /WEZ	CLD-S310F /WEZW/FR	CLD-S310S /WEZW/SP	
NSP	1	Front panel	VNK3191	VNK3191	VNK3195	VNK3196	
	12	Front panel assy-S	VXX2291	VXX2291	VXX2294	VXX2295	

(2) PARTS LIST FOR CLD-S310/WBW

Mark	No.	Description	Part No.
NSP	1	Front panel	VNK3191
	2	Pionner badge	PAM1608
	3	FL lens	VEC1791
	4	Key A	VNK2793
	5	LED lens	PNW2019
	6	PW button	VNK2329
	7	L key	VNK2812
	8	Main key	VNK3181
	9	Screw	BBZ30P080FMC
	10	FLKY assy	VWG1657
NSP	11	KEYB assy	VWG1627
	12	Front panel assy-S	VXX2291



2.5 BOTTOM VIEW SECTION

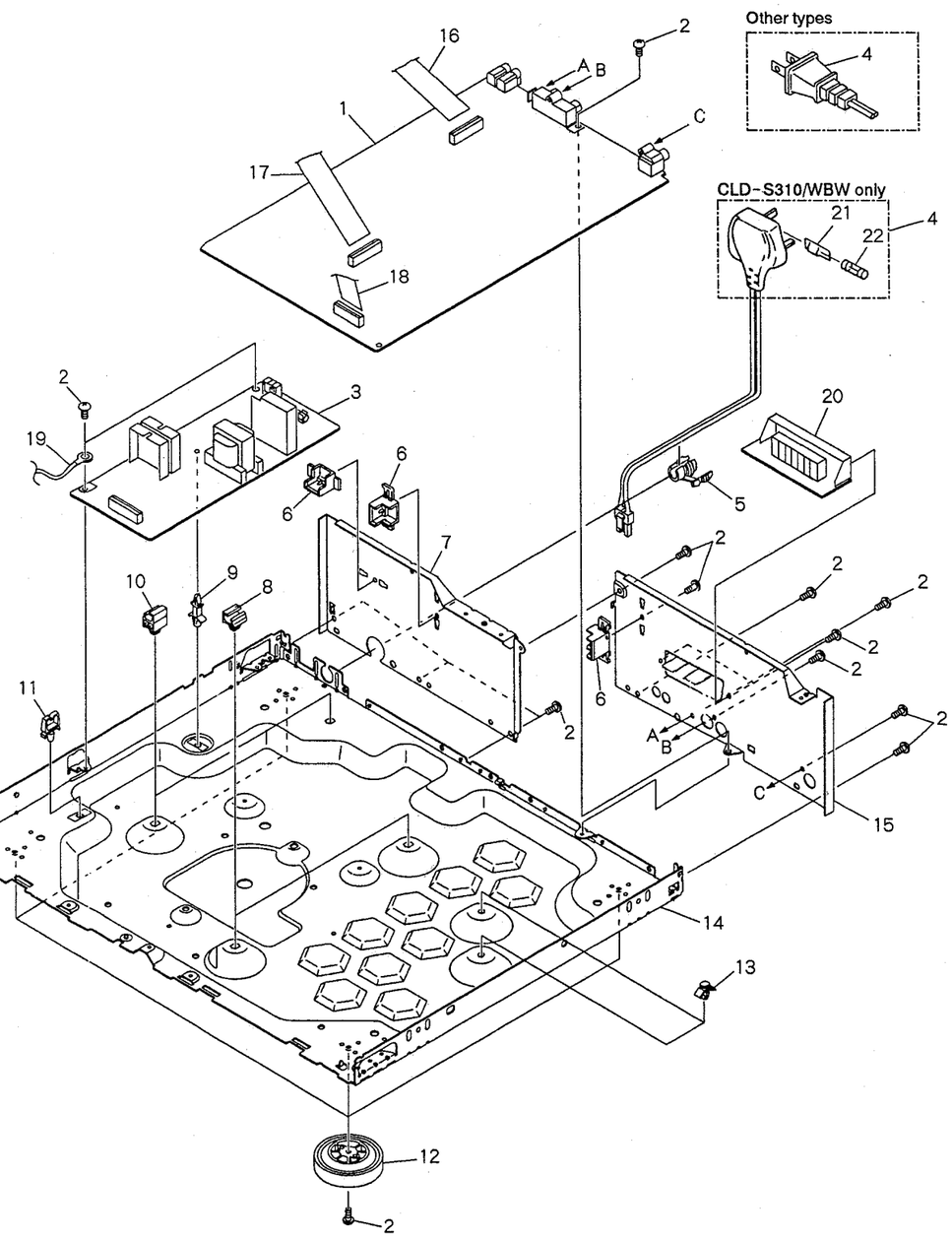
(1) CONTRAST OF CLD - S310/WBW, WEZ, CLD - S310F/WEZW/FR and CLD - S310S/WEZW/SP

CLD - S310/WBW, WEZ, CLD - S310F/WEZW/FR and CLD - S310S/WEZW/SP have the same construction except for the following:

Mark	No.	Symbol & Description	Part No.				Remarks
			CLD-S310 /WBW	CLD-S310 /WEZ	CLD-S310F /WEZW/FR	CLD-S310S /WEZW/SP	
⚠	4	AC power cord	VDG1063	VDG1061	VDG1061	VDG1061	
NSP	15	Rear panel L	VNA1573	VNA1573	VNA1580	VNA1581	
⚠	21	Fuse holder	VKR1003	Not used	Not used	Not used	
⚠	22	Fuse (5A)	PEK1003	Not used	Not used	Not used	

(2) PARTS LIST FOR CLD - S310/WBW

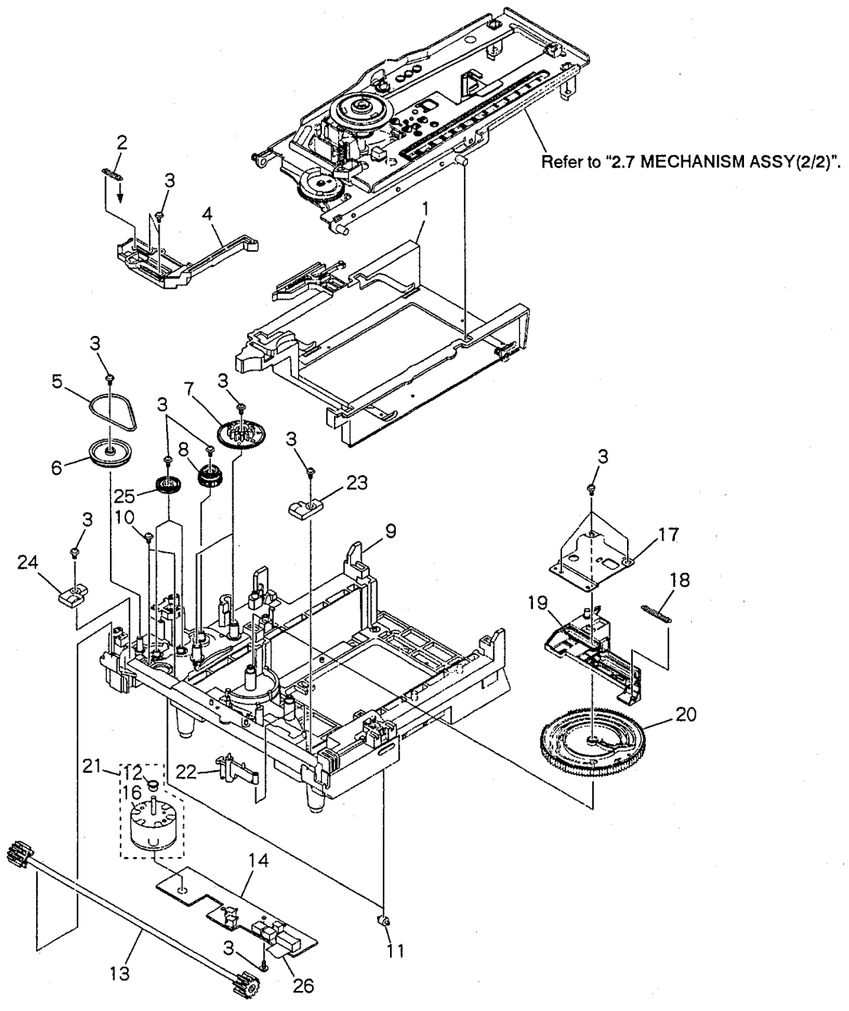
Mark	No.	Description	Part No.
	1	MOTHER assy	VWS1198
	2	Screw	BBZ30P080FMC
⚠	3	SYPS assy	VWR1234
⚠	4	AC power cord	VDG1063
⚠	5	Cord stopper	CM-22B
	6	Tray stopper	VNL1657
	7	Rear panel R	VNA1598
NSP	8	P plate holder	PNY-405
NSP	9	PC support	VEC-269
NSP	10	PCB hinge	VEC1174
NSP	11	Wire clip (H)	VEC1181
	12	Insulator	PNW1912
	13	Card spacer A	VEC1708
NSP	14	Base chassis	VNA1461
NSP	15	Rear panel L	VNA1573
	16	Flexible cable (23P)	VDA1464
	17	Flexible cable (21P)	VDA1465
	18	Flexible cable (16P)	VDA1469
NSP	19	Earth lead unit	XDF-507
NSP	20	SCRB assy	VWV1432
⚠	21	Fuse holder	VKR1003
⚠	22	Fuse (5A)	PEK1003



2.6 MECHANISM ASSY (1/2)

Parts List

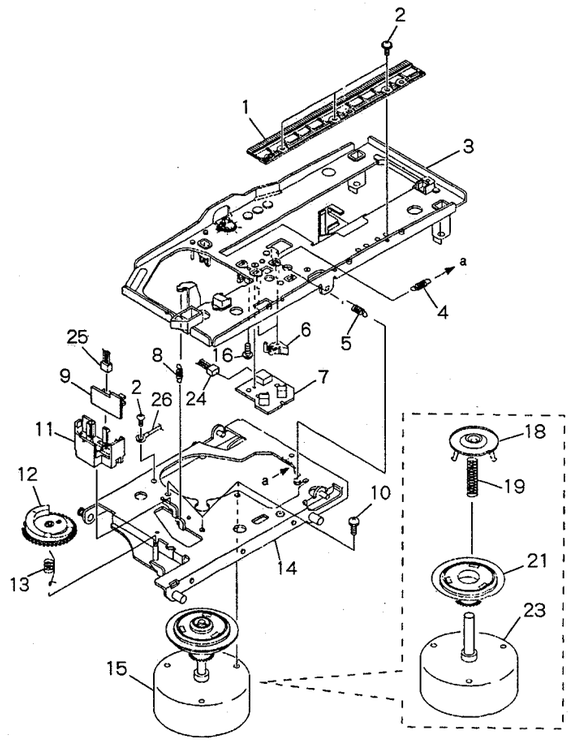
Mark	No.	Description	Part No.
	1	Clamp cam	VNL1633
	2	CDP spring	VBH1191
	3	Screw	Z39-019
	4	CD plate	VNL1632
	5	Rubber belt	VEB1184
	6	Gear pulley	VNL1662
	7	Twin gear	VNL1626
	8	Center gear	VNL1660
	9	Mechanism base	VNK3239
	10	Screw	BMZ26P040FMC
	11	Roller	VNL1042
NSP	12	Motor pulley	VNL1630
	13	Synchro gear assy	VXA2105
NSP	14	LMSB assy	VWG1554
	15	•••••	
NSP	16	Carriage motor	VXM1033
	17	Shaft holder	VNE1942
	18	CAS spring	VBH1190
	19	Cam plate	VNL1631
	20	Cam gear	VNL1625
	21	Loading motor assy	VXX2045
	22	MB-SW lever	VNL1664
	23	Slider (R)	VNL1666
	24	Slider (L)	VNL1665
	25	Double gear	VNL1661
	26	Flexible cable (10P)	VDA1466



2.7 MECHANISM ASSY (2/2)

Parts List

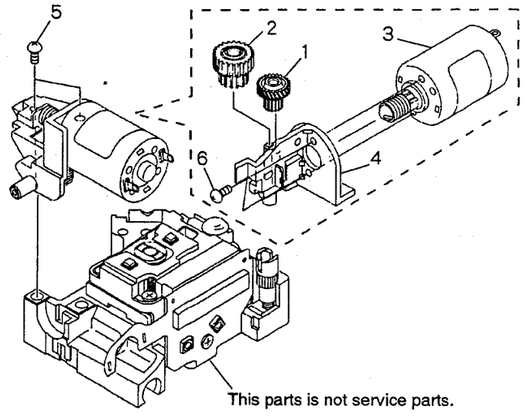
Mark	No.	Description	Part No.
	1	CA rack	VNL1647
	2	Screw	IBZ26P060FMC
	3	Tilt base	VNL1642
	4	Radial spring	VBH1246
	5	Thrust spring	VBH1245
	6	CA-switch lever	VNL1644
NSP	7	PKSB assy	VWG1555
	8	Tilt tension spring	VBH1244
NSP	9	FG assy	VWG1556
	10	Screw	PMA30P050FMC
	11	FG base	VNL1645
	12	Tilt cam	VNL1643
	13	Tilt cam spring	VBH1243
	14	Motor base	VNE1941
	15	Spindle motor assy	VXA2125
	16	Screw	IBZ26P120FMC
	17	•••••	
	18	Centering hab	VNL1623
	19	Centering spring	VBH1083
	20	•••••	
NSP	21	Turn table assy	VXA2116
	22	•••••	
NSP	23	Spindle motor	VXM1057
	24	Housing assy (3P:blue)	VKP2045
	25	Housing assy (3P:yellow)	VKP2046
NSP	26	Earth lead unit	XDF-507



2.8 CARRIAGE ASSY

Parts List

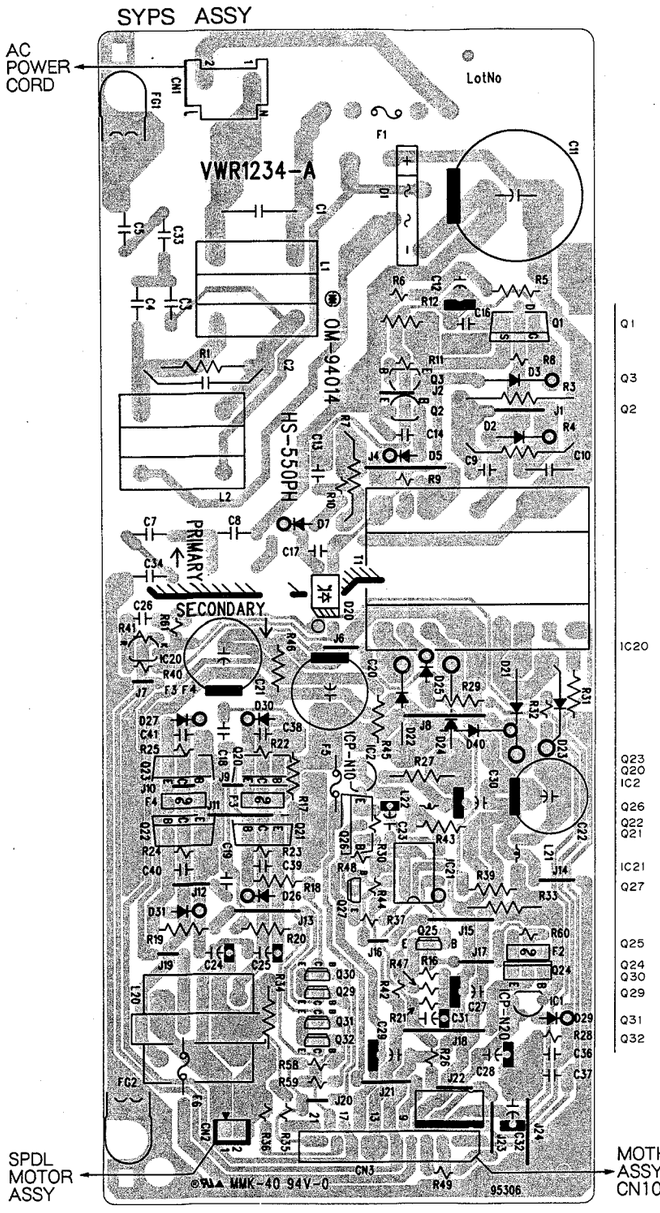
Mark	No.	Description	Part No.
	1	CA gear (A)	VNL1638
	2	CA gear (B)	VNL1639
	3	Slider motor assy	VXX2082
	4	Motor holder	VNL1700
	5	Screw	PBZ20P050FMC
	6	Screw	PMZ20P030FMC

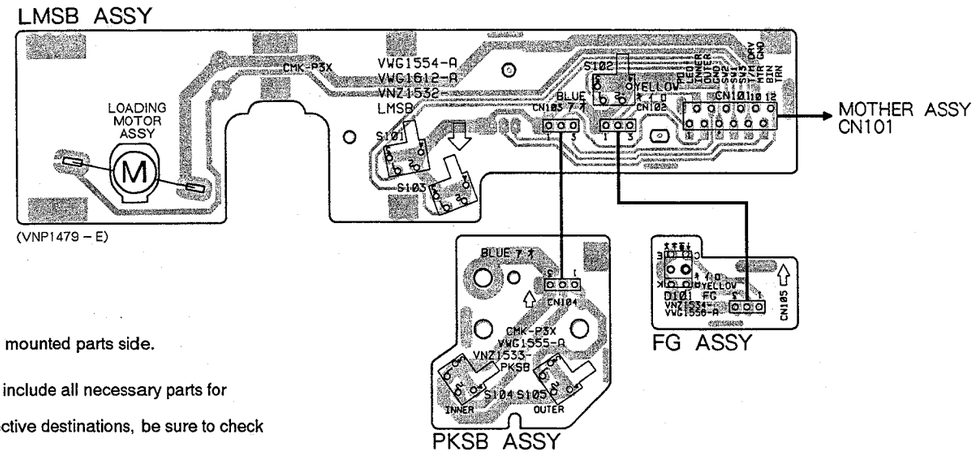


3. SCHEMATIC AND PCB CONNECTION DIAGRAMS

3.1 OVERALL CONNECTIONS, KEYB, FLKY, SYPS, PKSB, FG, LMSB AND CARRIAGE ASSEMBLIES

PCB – 1

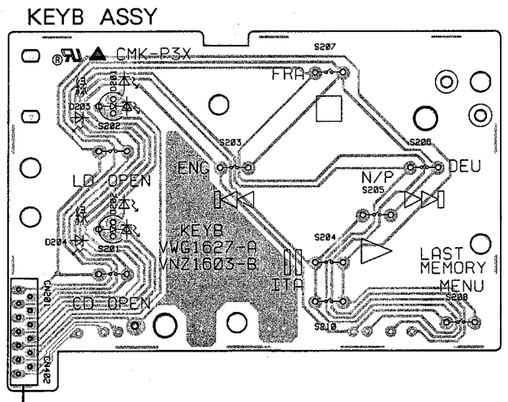


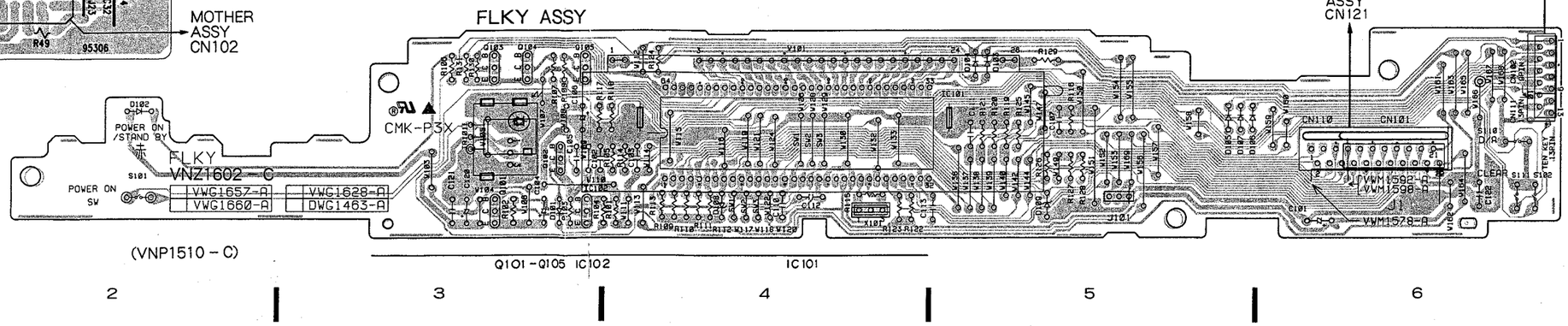


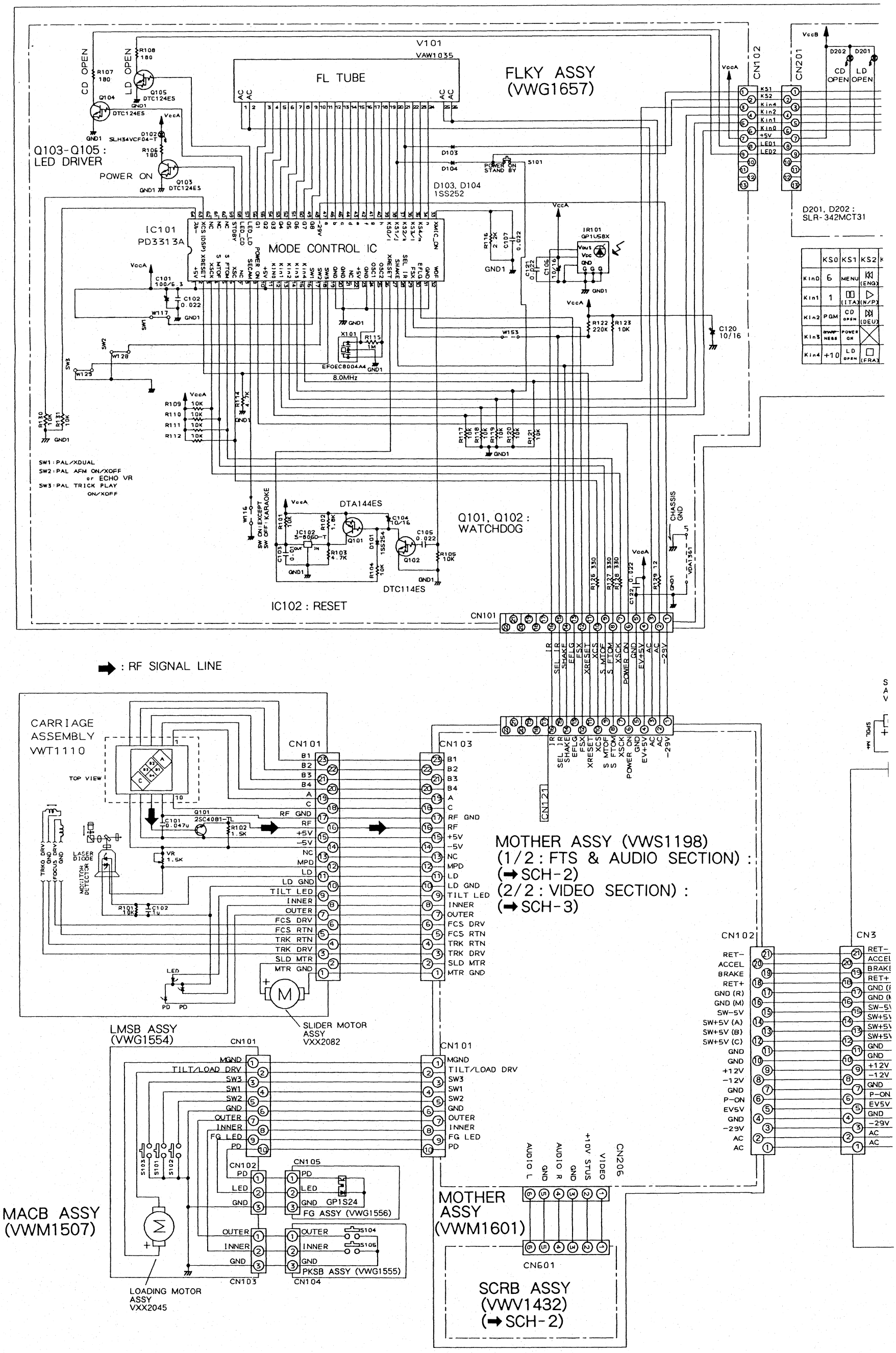
- This diagram is viewed from the mounted parts side.
- The parts mounted on this PCB include all necessary parts for several destinations.
  For further information for respective destinations, be sure to check with the schematic diagram.

NOTE FOR PCB DIAGRAMS:
1. Part numbers in PCB diagrams match those in the schematic diagrams.
2. A comparison between the main parts of PCB and schematic diagrams is shown below.

Symbol in PCB Diagrams	Symbol in Schematic Diagrams	Part Name
B C E	B C E B C E	Transistor
B C E	B C E B C E	Transistor with resistor
D G S	D G S D G S	Field effect transistor
		Resistor array
		3-terminal regulator





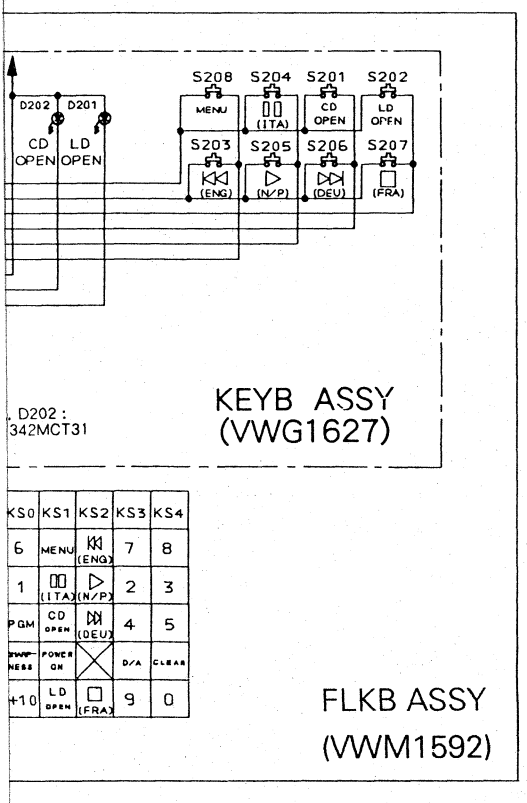


	KS0	KS1	KS2	K
Kin0	6	MENU	⏮ (ENG)	
Kin1	1	▯▯ (ITA)	▷ (N/P)	
Kin2	PGM	CD OPEN	⏭ (DEU)	
Kin3	SHARPNESS	POWER ON		
Kin4	+10	LD OPEN	□ (FRA)	

SCH-1 OVERALL CONNECTIONS, KEYB ASSY, FLKY ASSY, SYPS ASSY, PKSB ASSY, FG ASSY, LMSB ASSY, CARRIAGE ASSY

CLD - S310, CLD - S31
CLD - S310S

SCH – 1



NOTE FOR SCHEMATIC DIAGRAMS

(Type 4A)

1. **When ordering service parts, be sure to refer to "PARTS LIST of EXPLODED VIEWS" or "PCB PARTS LIST".**

2. **Since these are basic circuits, some parts of them or the values of some components may be changed for improvement.**

3. **RESISTORS:**
   Unit: k:kΩ, M:MΩ, or Ω unless otherwise noted.
   Rated power: 1/4W, 1/6W, 1/8W, 1/10W unless otherwise noted.
   Tolerance:(F):±1%, (G):±2%, (K):±10%, (M):±20% or ±5% unless otherwise noted.

4. **CAPACITORS:**
   Unit : p:pF or μF unless otherwise noted.
   Ratings : capacitor (μF) / voltage (V) unless otherwise noted.
   Rated voltage : 50V except for electrolytic capacitors.

5. **COILS:**
   Unit : m:mH or μH unless otherwise noted.

6. **VOLTAGE AND CURRENT:**
   ▭ or ←V :
   DC voltage (V) in PLAY mode unless otherwise noted.
   ⇦mA or ←mA :
   DC current in PLAY mode unless otherwise noted.
   Value in ( ) is DC current in STOP mode.

7. **OTHERS:**
   - ⊘ or ⊘ : Adjusting point.
   - ⩤ : Measurement point.
   - The ⚠ mark found on some component parts indicates the importance of the safety factor of the parts. Therefore, when replacing, be sure to use parts of identical designation.

8. **SCH – □ ON THE SCHEMATIC DIAGRAM:**
   - SCH–□ indicates the drawing number of the schematic diagram. (SCH stands for schematic diagram.)

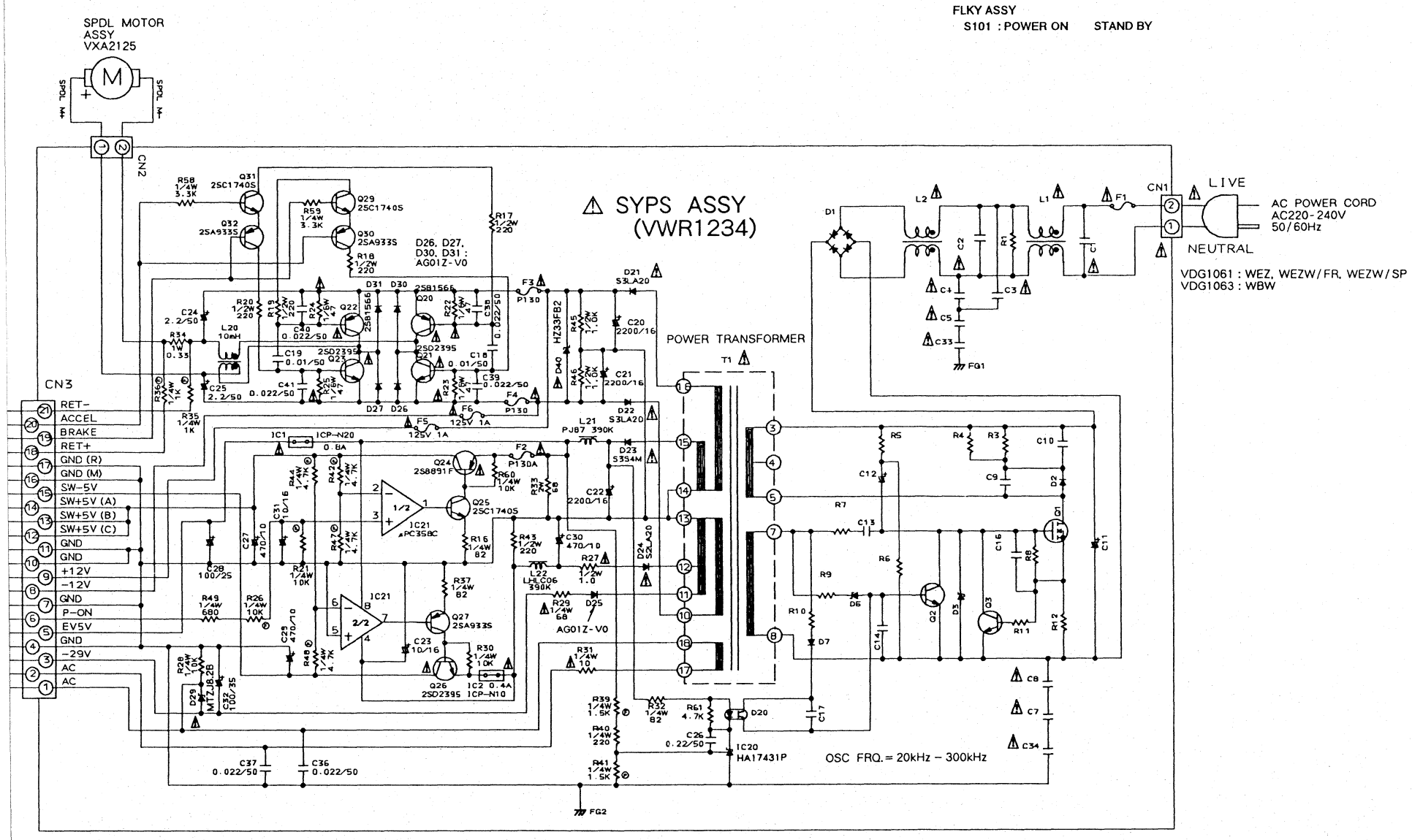
9. **SWITCHES** (Underline indicates switch position):

LMSB ASSY
S101 : SW1
S102 : SW2
S103 : SW3

PKSB ASSY
S104 : OUTER SW
S105 : INNER SW

KEYB ASSY
S201 : CD OPEN/CLOSE (⏏)
S202 : LD OPEN/CLOSE (⏏)
S203 : ⏮
S204 : ⏸
S205 : ▶
S206 : ⏭
S207 : ■
S208 : MENU

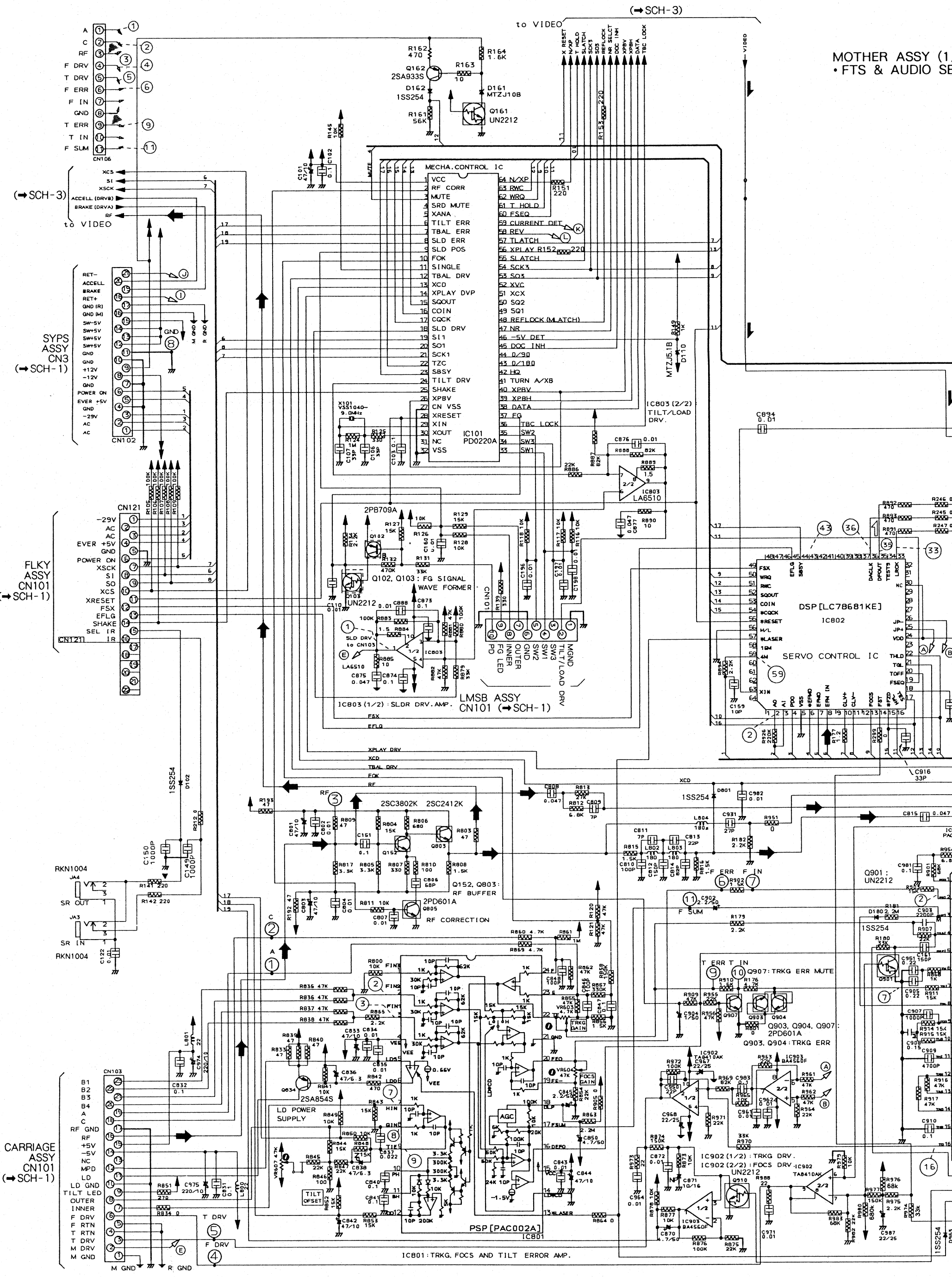
FLKY ASSY
S101 : POWER ON STAND BY



OVERALL CONNECTIONS, KEYB ASSY, FLKY ASSY, SYPS ASSY, PKSB ASSY, FG ASSY, LMSB ASSY, CARRIAGE ASSY

SCH-1

3.2 MOTHER ASSY (1/2 : FTS AND AUDIO SECTION) AND SCRB ASSY



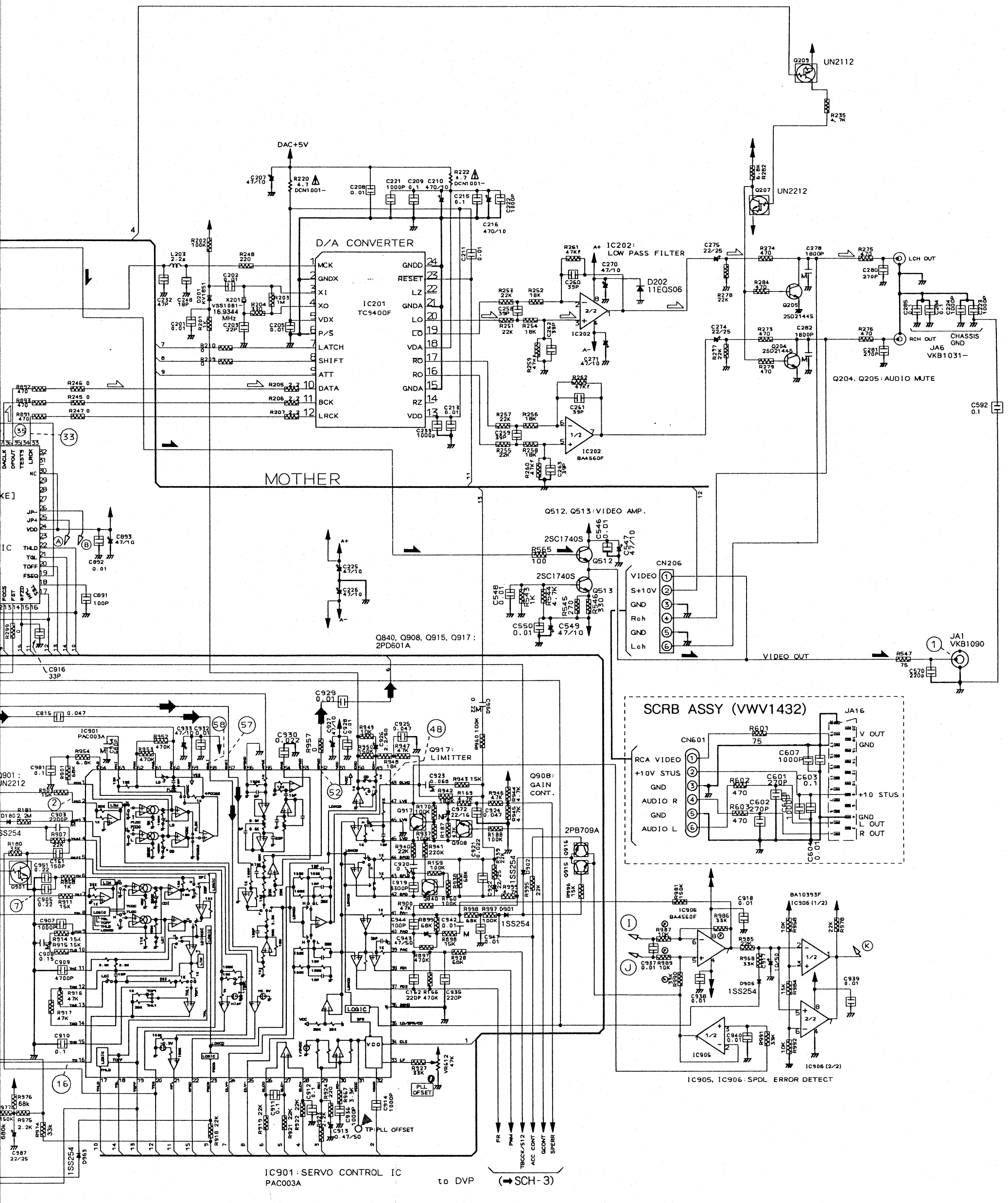
SCH-2 MOTHER ASSY (1/2), SCRB ASSY

HER ASSY (1/2) (VWS1198)
& AUDIO SECTION

SCH – 2

J10 J10
+5V ① ① +5V
GND ② ② GND
+12V ③ ③ +12V
–12V ④ ④ –12V

: RF SIGNAL LINE
: DIGITAL AUDIO SIGNAL LINE
: VIDEO SIGNAL LINE



MOTHER ASSY (1/2), SCRB ASSY **SCH-2**

WAVEFORMS AND VOLTAGE

FTS AND AUDIO SECTION

Note : (No.) in the table correspond to the pin number.

Measurement condition : In case when (D. audio) is written, at time when disc that has digital audio recording is played.

IC801(PAC002A)	IC802(LC78681KE)	IC803(LA6510)	IC901(PAC003A)	CN106	Video output pin
②, ③ 1mS/Div. 16mVp-p AC mode	② 0.1μS/Div. 4.3Vp-p AC mode(D.audio)	① 2mS/Div. 1.8Vp-p 0V DC mode	② 0.2mS/Div. 74mVp-p 0V DC mode	①, ② 5mS/Div. 65mVp-p 0V DC mode	① approx. 1Vp-p (75Ω termination) V : 20mV/Div H : 10mS/Div
⑦, ⑧ 1mS/Div. 67mVp-p 0V DC mode	㉝ 10μS/Div. 4.2Vp-p AC mode(D.audio)		⑦ 0.2mS/Div. 74mVp-p 0V DC mode	③ 0.5mS/Div. 300mVp-p AC mode	
⑨ 5mS/Div. 0.1Vp-p 0V DC mode	㉟ 0.2μS/Div. 4.4Vp-p AC mode(D.audio)		⑯ 0.2mS/Div. 0.61Vp-p 0V DC mode	④ 5mS/Div. 15Vp-p 0V DC mode	
	㊱ 0.2μS/Div. 4.5Vp-p AC mode(D.audio)		㊽ 50μS/Div. 6.2Vp-p 0V DC mode	⑤ 5mS/Div. 5.8Vp-p 0V DC mode	
	㊸ 0.1μS/Div. 4.5Vp-p AC mode(D.audio)		㊷ 0.2μS/Div. 2.1Vp-p AC mode	⑥ 5mS/Div. 3.5Vp-p 0V DC mode	
	㊾ 0.1μS/Div. 2Vp-p AC mode(D.audio)		㊼ 1mS/Div. 0.53Vp-p 0V DC mode	⑨ 5mS/Div. 1.25Vp-p 0V DC mode	
			㊽ 0.2mS/Div. 0.32Vp-p 0V DC mode	⑪ 10mS/Div. 1.7Vp-p DC mode	

MOTHER ASSY

SCRB ASSY

CARRIAGE ASSY CN101

VWV1432-A

VWS1197-A VWS0000-0 VWS0000-0

VWS1196-A DWS1249-A VWS0000-0 VWS0000-0

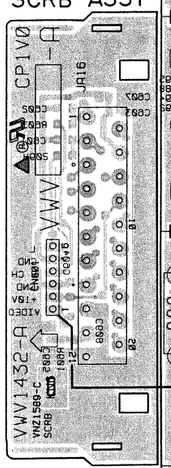
VR608 VR607 VR603 VR604 VR450

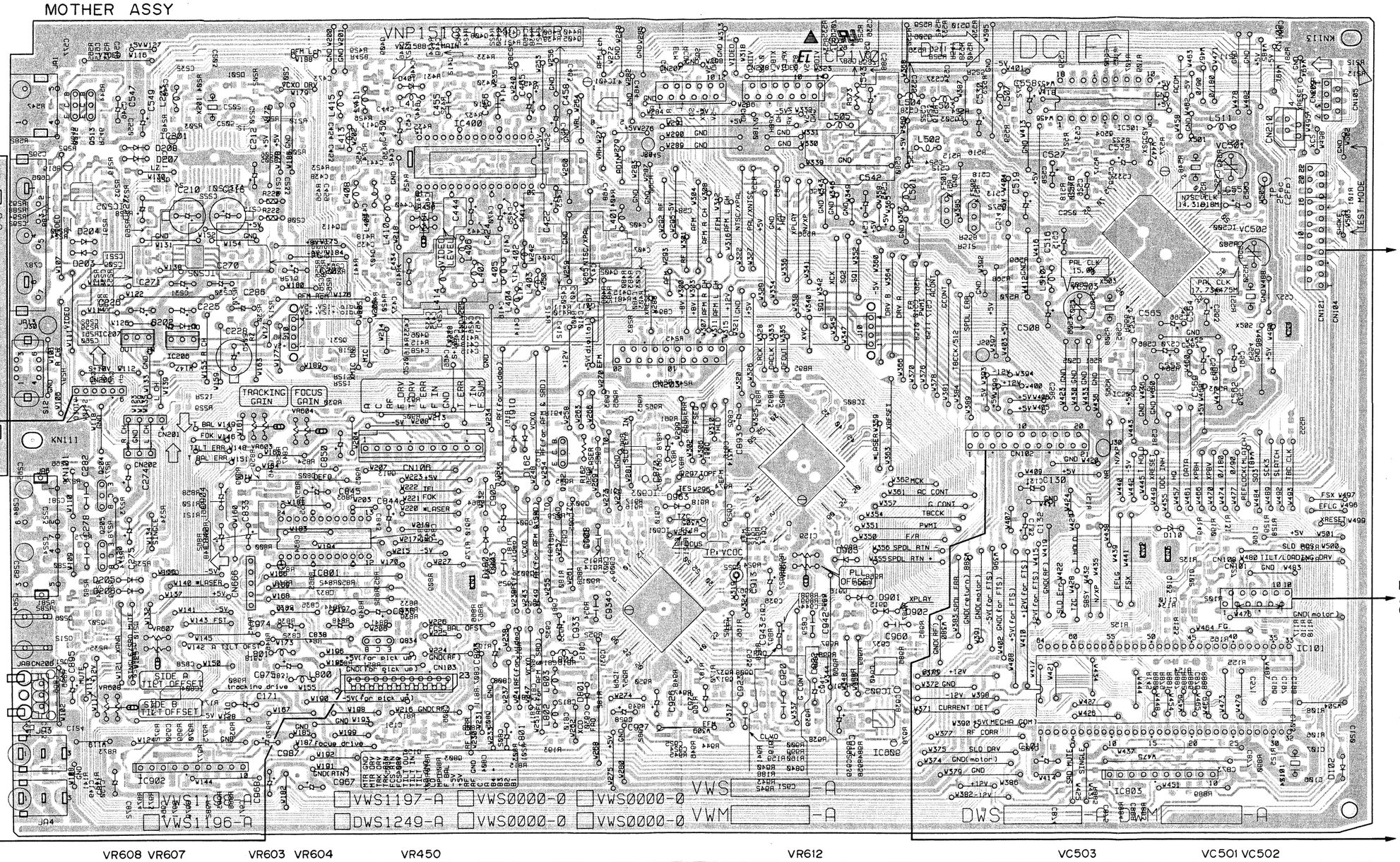
● This diagram is viewed from the r

PCB – 2

MOTHER ASSY

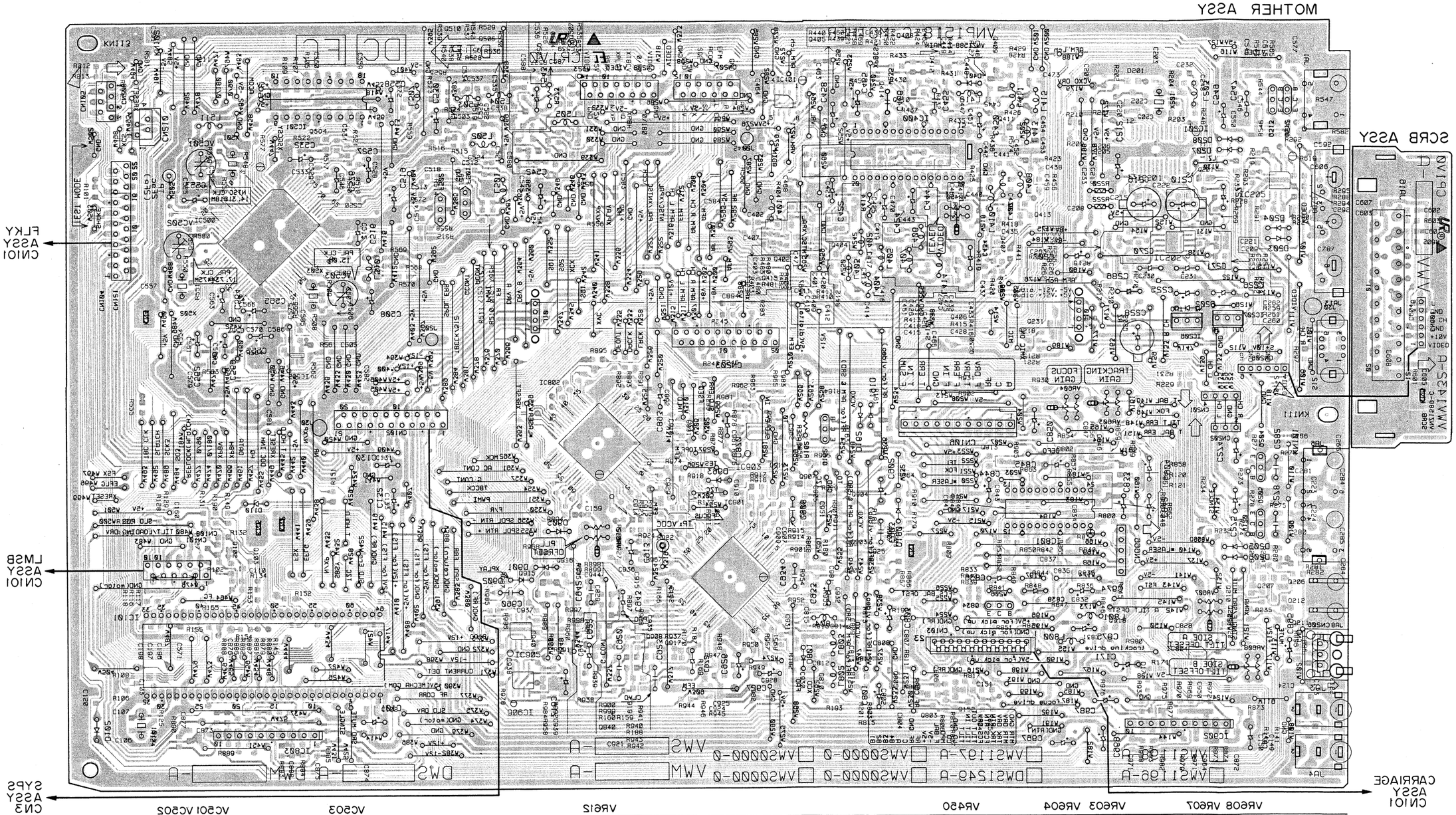
SCRB ASSY



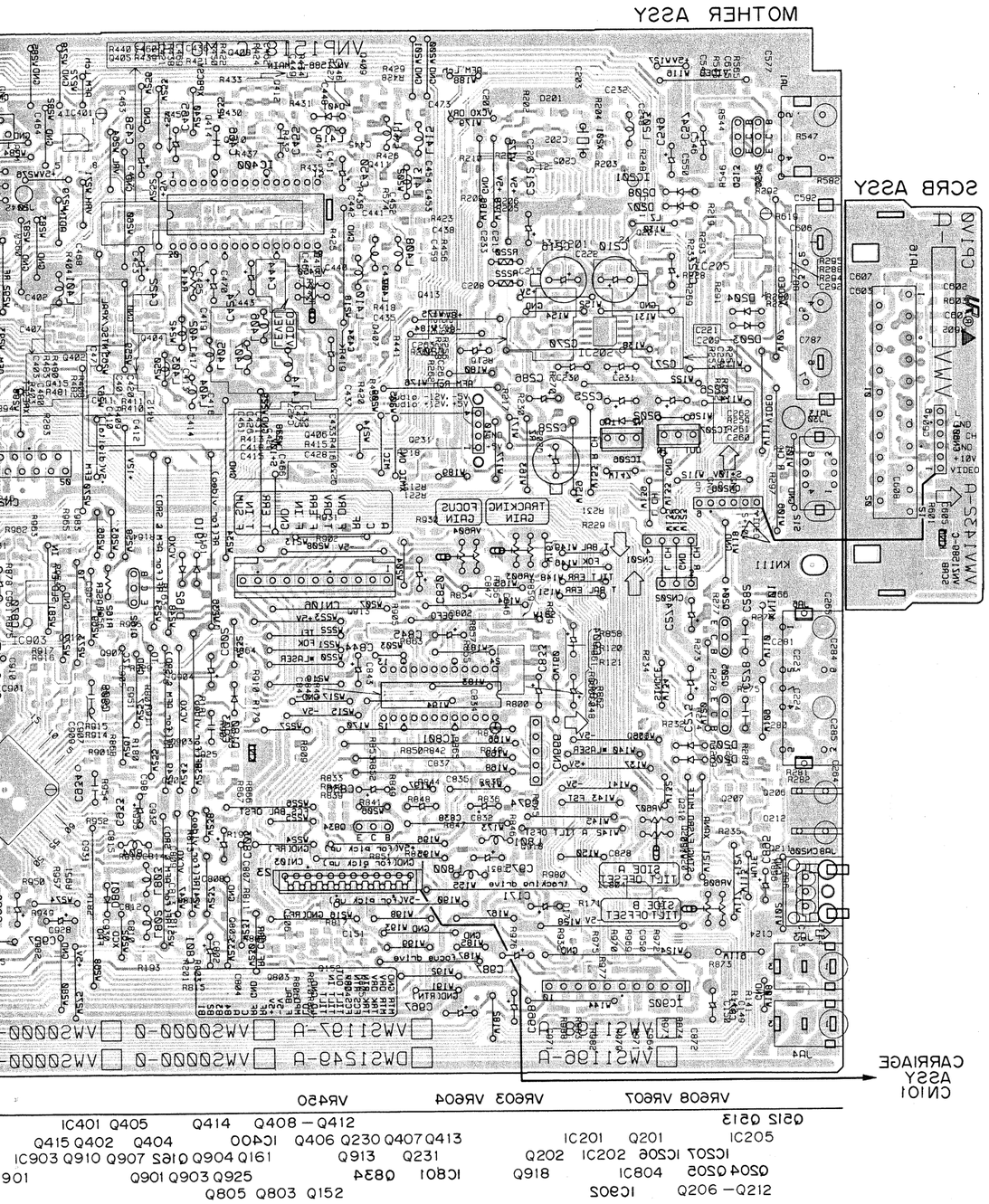


- This diagram is viewed from the mounted parts side.
- The parts mounted on this PCB include all necessary parts for several destinations.
  For further information for respective destinations, be sure to check with the schematic diagram.

CLD – S310, CLD – S310F,
CLD – S310S



● This diagram is viewed from the foil side.



m is viewed from the foil side.

WAVEFORMS AND VOLTAGE

VIDEO SECTION

Note : (No.) in the table correspond to the pin number.

Measurement condition : In case when (D. audio) is written, at time when disc that has digital audio recording is played.

IC400 (PAC005B)

(10) 1.52Vp-p, 0.55V — V : 20mV/Div, H : 10mS/Div

(8) (TOP) 2.4V — (11) (BOTTOM) 1.85V, 0.55V

(12) 1Vp-p, 1.65V — V : 20mV/Div, H : 10mS/Div

(14) 1Vp-p — V : 20mV/Div, H : 10mS/Div

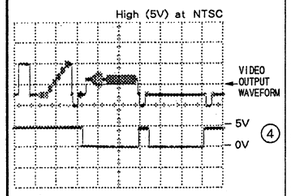
(22) (No noise)

(25) (with limiter noise) — V : 20mV/Div, H : 10mS/Div, approx. 330mVp-p

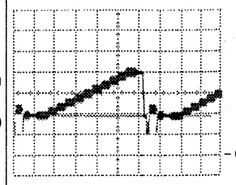
(27) approx. 1Vp-p — 0.5mS/Div

IC500 (PD6159A)

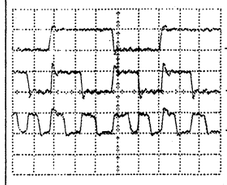
(4) XTBCV (at PAL) V : 0.5V/Div H : 20µS/Div



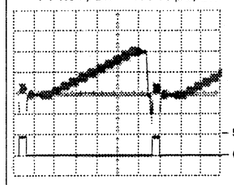
(37) ADIN (at PAL) V : 0.5V/Div H : 10µS/Div



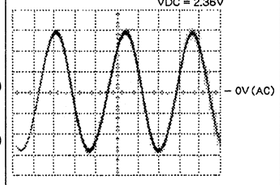
(58) DC02 (60) DC05 (61) DC07 V : 0.5V/Div H : 50nS/Div



(37) ADIN (at PAL)
(45) PBCLP (PILOT BURST CLAMP PULSE) V : 0.5V/Div H : 10µS/Div



(64) AD CKP (at PAL) (15.0MHz) V : 50mV/Div H : 20nS/Div



(22) RCK/XRCK (at PAL BLUE BACK) 4fsc = 17.734475MHz V : 0.5V/Div H : 50nS/Div

(41) XPB CSY (X PLAY BACK COMPOSITE SYNC) V : 0.5V/Div H : 10µS/Div

(70) DC01 (at PAL) (3.75MHz) V : 10mV/Div H : 0.1µS/Div

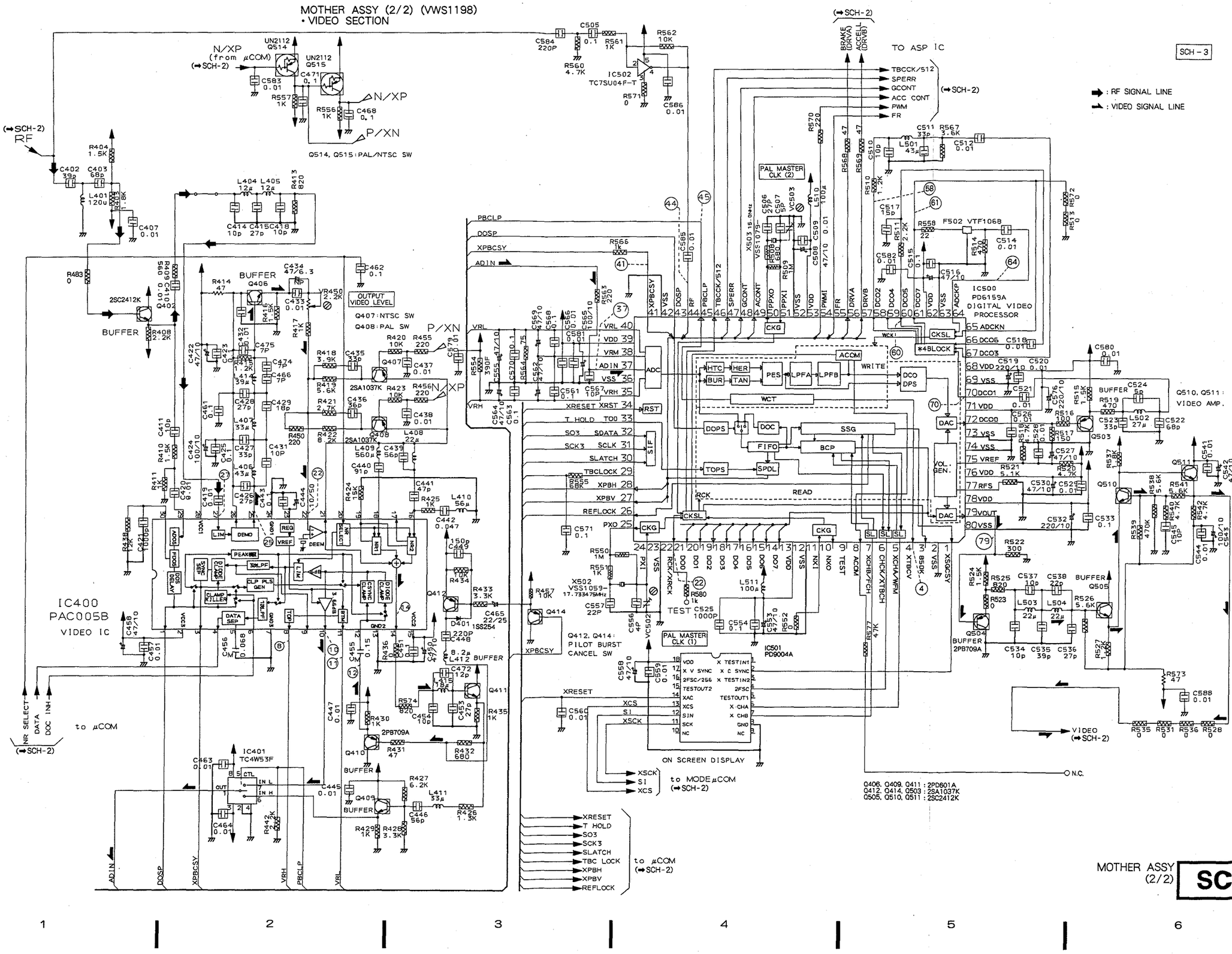
(22) RCK/XRCK (at PAL DISC PLAY) 4fp = 15.0MHz V : 0.5V/Div H : 50nS/Div

(44) RF (at PLAY) V : 0.1V/Div H : 5mS/Div
2.2VDC at PLAY
2.4VDC at STOP

(79) VOUT (D/A OUT) V : 20mV/Div H : 10µS/Div

Pin	VDC (V)
35	2.40
38	1.475
40	0.55
75	2.5
77	2.5

3.3 MOTHER ASSY (2/2 : VIDEO SECTION)



4. PCB PARTS LIST

NOTES:

- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*
- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

Ex.1 When there are 2 effective digits(any digit apart from 0), such as 560 ohm and 47k ohm(tolerance is shown by J=5%, and K=10%).

560 Ω → 56 × 10¹ → 561 ····· RD1/8PM 5 6 1 J
47k Ω → 47 × 10³ → 473 ····· RD1/4PS 4 7 3 J
0.5 Ω → 0R5 ····· RN2H 0 R 5 K
1 Ω → 010 ····· RS1P 0 1 0 K

Ex.2 When there are 3 effective digits(such as in high precision metal film resistors).

5.62k Ω → 562 × 10¹ → 5621 ····· RN1/4PC 5 6 2 1 F

Mark	No.	Description	Part No.
LIST OF ASSEMBLIES			
NSP		MACB ASSY	VWM1507
NSP		├LMSB ASSY	VWG1554
NSP		├PKSB ASSY	VWG1555
NSP		└FG ASSY	VWG1556
NSP		FLKB ASSY	VWM1592
NSP		├KEYB ASSY	VWG1627
		└FLKY ASSY	VWG1657
		MOTHER ASSY	VWM1601
		├MOTHER ASSY	VWS1198
NSP		└SCRB ASSY	VWV1432
⚠		SYPS ASSY	VWR1234
MACB ASSY			
OTHERS			
		PC board MACB	VNP1479
LMSB ASSY			
SWITCHES			
	S101-S103		DSG1017
OTHERS			
	CN101	10P FFC CONNECTOR	52044-1045
PKSB ASSY			
SWITCHES			
	S104, S105		DSG1017
FG ASSY			
SEMICONDUCTOR			
	D101		GP1S24

Mark	No.	Description	Part No.
FLKB ASSY			
OTHERS			
		PC board FLKB	VNP1510
KEYB ASSY			
SEMICONDUCTORS			
	D201, D202		SLR-342MCT31
SWITCHES			
	S201, S202, S205, S208		RSG1030
	S203, S204, S206, S207		RSG1034
OTHERS			
	CN201	1.25FJ CONNECTOR	09P-1.25FJ
FLKY ASSY			
SEMICONDUCTORS			
	IC101		PD3313A
	IC102		S-806D
	Q101		DTA144ES
	Q102		DTC114ES
	Q103-Q105		DTC124ES
	D103, D104		1SS252
	D101		1SS254
	D102		SLH34VCF04
SWITCH			
	S101		RSG1030
CAPACITORS			
	C104, C106, C120		CEAL100M16
	C101		CEAL101M6R3
	C103		CKPUYF103Z25
	C102, C105, C107, C121, C122		CKPUYF223Z25
RESISTORS			
	All Resistors		RD1/6PM□□□J

Mark	No.	Description	Part No.
OTHERS			
	CN102	1.25FJ CONNECTOR	09R-1.25FJ
	CN101	FFC BOTTOM CONNECTOR 16P	52492-1620
	X101	CERAMIC RESONATOR(8.0MHz)	EFOEC8004A4
	IR101	REMOTE SENSOR	GP1U58X
	V101	FL TUBE	VAW1035
		SPACER	VEC1599
		FL HOLDER	VNF1085
MOTHER ASSY			
SEMICONDUCTORS			
	IC906		BA10393F
	IC202, IC903, IC905		BA4560F
	IC803		LA6510
	IC802		LC78681KE
	IC801		PAC002A
	IC901		PAC003A
	IC400		PAC005B
	IC101		PD0220A
	IC500		PD6159A
	IC501		PD9004A
	IC902		TA8410AK
	IC401		TC4W53F
	IC502		TC7SU04F
	IC201		TC9400F
	Q102, Q410, Q504, Q916		2PB709A
	Q406, Q409, Q411, Q805, Q840		2PD601A
	Q903, Q904, Q907, Q908, Q915		2PD601A
	Q917		2PD601A
	Q407, Q408, Q412, Q414, Q503		2SA1037K
	Q834		2SA854S
	Q162		2SA933S
	Q512, Q513		2SC1740S
	Q402, Q505, Q510, Q511, Q803		2SC2412K
	Q152		2SC3802K
	Q204, Q205		2SD2144S
	Q209, Q514, Q515		UN2112
	Q103, Q161, Q207, Q901, Q910		UN2212
	D202		11EQS06
	D102, D162, D180, D401, D801		1SS254
	D901, D902, D905, D963		1SS254
	D201		KV1851
	D161		MTZJ10B
	D110		MTZJ5.1B
COILS AND FILTER			
	L510, L511		LAU101J
	L404, L405		LAU120J
	L401		LAU121J
	L415		LAU180J
	L802-L804		LAU181J
	L408, L503, L504, L800, L801		LAU220J
	L502		LAU270J
	L203		LAU2R2J
	L407, L411		LAU330J
	L414		LAU390J

Mark	No.	Description	Part No.
	L406, L501		LAU430J
	L410		LAU560J
	L412		LAU8R2J
	L409		LFA561J
	F502		VTF1068
CAPACITORS			
	C556		CCSQCH040C50
	C507, C524		CCSQCH050C50
	C466, C474, C475, C809, C811		CCSQCH070D50
	C159, C411, C414, C418, C431		CCSQCH100D50
	C454, C510, C534, C537, C545		CCSQCH100D50
	C567		CCSQCH100D50
	C810, C846, C848, C891, C944		CCSQCH101J50
	C472		CCSQCH120J50
	C517		CCSQCH150J50
	C161, C449, C812		CCSQCH151J50
	C248, C429		CCSQCH180J50
	C203, C538, C557, C813, C950		CCSQCH220J50
	C162, C448, C577, C584, C935		CCSQCH221J50
	C415, C426, C428, C473, C506		CCSQCH270J50
	C536, C931		CCSQCH270J50
	C280, C281		CCSQCH271J50
	C106, C107, C427, C435, C511		CCSQCH330J50
	C523, C916		CCSQCH330J50
	C436		CCSQCH360J50
	C258-C263, C402, C535		CCSQCH390J50
	C232, C441		CCSQCH470J50
	C439, C446		CCSQCH560J50
	C403, C522, C806		CCSQCH680J50
	C814		CCSQCH820J50
	C440		CCSQCH910J50
	C836		CEAL470M6R3
	C838		CEALNP470M6R3
	C871		CEANP100M16
	C972		CEANP220M16
	C434		CEANP470M6R3
	C904		CEAS010M50
	C444, C917		CEAS100M50
	C424, C543, C565		CEAS101M10
	C274, C275, C465, C922		CEAS220M25
	C967, C968, C987		CEAS220M25
	C519, C532, C576, C974, C975		CEAS221M10
	C845, C902, C926		CEAS2R2M50
	C101, C207, C225, C226		CEAS470M10
	C270, C271, C422, C450, C458		CEAS470M10
	C508, C516, C527, C530, C542		CEAS470M10
	C547, C549, C553, C555, C558		CEAS470M10
	C562, C564, C569, C801, C803		CEAS470M10
	C833, C842, C844, C893, C927		CEAS470M10
	C933		CEAS470M10
	C210, C216		CEAS471M10
	C850, C870		CEAS4R7M50
	C913, C943		CEASR47M50
	C149, C150, C220-C224, C233		CKSQYB102K50
	C421, C525, C907, C914, C936		CKSQYB102K50
	C919		CKSQYB332K50

Mark	No.	Description	Part No.
	C909		CKSQYB472K50
	C110, C122, C160, C196-C198		CKSQYF103Z50
	C201, C202, C205, C208, C211		CKSQYF103Z50
	C213, C407, C410, C419, C420		CKSQYF103Z50
	C432, C433, C437, C438, C445		CKSQYF103Z50
	C447, C457, C463, C464, C509		CKSQYF103Z50
	C512, C514, C518, C520, C521		CKSQYF103Z50
	C526, C528, C529, C541, C544		CKSQYF103Z50
	C546, C548, C550, C559, C560		CKSQYF103Z50
	C566, C579-C583, C585, C586		CKSQYF103Z50
	C588, C802, C804, C807		CKSQYF103Z50
	C834, C835, C843, C872, C876		CKSQYF103Z50
	C888, C892, C894, C918		CKSQYF103Z50
	C928, C929, C932, C937-C939		CKSQYF103Z50
	C941, C961, C962, C964, C971		CKSQYF103Z50
	C982		CKSQYF103Z50
	C102, C103, C151, C209, C215		CKSQYF104Z25
	C284, C285, C423, C425, C443		CKSQYF104Z25
	C451, C461, C462, C468, C471		CKSQYF104Z25
	C505, C515, C533, C554, C561		CKSQYF104Z25
	C563, C568, C570, C571, C592		CKSQYF104Z25
	C831, C832, C840, C841, C847		CKSQYF104Z25
	C873, C874, C910-C912, C940		CKSQYF104Z25
	C981, C983		CKSQYF104Z25
	C837, C921, C930		CKSQYF223Z50
	C905, C951		CKSQYF224Z25
	C442, C808, C815, C875, C877		CKSQYF473Z25
	C924, C925		CKSQYF473Z25
	C942		CQMA103J50
	C920		CQMA104J50
	C455, C908		CQMA154J50
	C278, C282		CQMA182J50
	C903		CQMA222J50
	C960		CQMA224J50
	C934		CQMA681J50
	C456, C923		CQMA683J50
	VC502, VC503 (20pF)		VCM-008
RESISTORS			
⚠	R220, R222 (4.7Ω, 1/6W)		DCN1001
	R414, R573		RD1/6PM470J
	R162		RD1/6PM471J
	R987, R989		RN1/10SE103D
	R986, R990		RN1/10SE333D
	R554		RN1/10SE391D
	R259-R262		RN1/10SE473D
	VR450	(2.2kΩ)	RCP1019
	VR603	(4.7kΩ)	RCP1020
	VR604, VR607, VR612	(47kΩ)	RCP1047
	Other Resistors		RS1/10S□□□J
OTHERS			
		4P CABLE HOLDER	51048-0400
	CN101	10P FFC CONNECTOR	52045-1045
	CN121	16P FFC CONNECTOR	52045-1645
	CN102	21P FFC CONNECTOR	52045-2145
	CN103	23P FFC CONNECTOR	52233-2310

Mark	No.	Description	Part No.
	CN106	11P TOP POST	B11P-SHF-1AA
	CN206	KR CONNECTOR	B6B-PH-K-S
	JA3, JA4	REMOTE CONTROL JACK	RKN1004
		PCB BINDER	VEF1040
	JA6	2P PIN JACK	VKB1031
	JA1	1P PIN JACK	VKB1090
		SCREW TERMINAL	VNE1948
	KN101, KN102	EARTH PLATE	VNF1084
	X101	CERAMIC RESONATOR(9.0MHz)	VSS1040
	X502	CRYSTAL RESONATOR(17.734MHz)	VSS1059
	X503	CRYSTAL RESONATOR(15.0MHz)	VSS1079
	X201	CRYSTAL RESONATOR(16MHz)	VSS1081

SCRB ASSY

CAPACITORS

	C601, C602		CCSQCH271J50
	C607, C608		CKSQYB102K50
	C604		CKSQYF103Z50
	C603		CKSQYF104Z25

RESISTORS

	All Resistors		RS1/10S□□□J

OTHERS

	CN601	KR CONNECTOR	B6B-PH-K-S
		PCB BINDER	VEF1040
	JA16	RGB CONNECTOR	VKB1037

SYPS ASSY

SEMICONDUCTORS

⚠	IC1		ICP-N20
⚠	IC2		ICP-N10
	IC20		HA17431P
	IC21		UPC358C
	Q27, Q30, Q32		2SA933S
⚠	Q20, Q22		2SB1566
⚠	Q24		2SB891F
	Q25, Q29, Q31		2SC1740S
⚠	Q21, Q23, Q26		2SD2395
	D25-D27, D30, D31		AG01Z-V0
⚠	D29		MTZJ8.2B
⚠	D40		RD33FB2
⚠	D24		S2LA20
⚠	D21, D22		S3LA20
⚠	D23		S3S4M

RESISTORS

⚠	R22-R25	(47Ω, 1/6W)	VCN1033
⚠	R27	(1Ω, 1/2W)	VCN1047
⚠	R31	(10Ω, 1/4W)	VCN1051
⚠	R29	(68Ω, 1/4W)	VCN1052

OTHERS

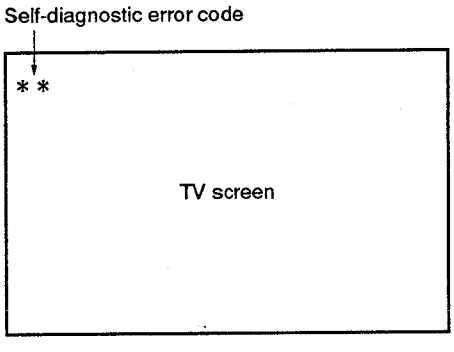
⚠	F2	FUSE	VEK1033
⚠	F3, F4	FUSE	VEK1034
⚠	F5, F6	FUSE(1.0A/125V)	VEK1036

5. SELF-DIAGNOSTIC FUNCTIONS

5.1 SELF-DIAGNOSTIC FUNCTIONS

The self-diagnostic functions automatically display an error code on the TV screen and front panel fluorescent display section when there is an error. The customer checks the error code and conveys it to the service personnel to make repairs more efficient.

After an error occurs, even if the error code goes off, you can display the error code again by holding down the CLEAR key for 10 seconds (except a loading error L * display). However, if the power cord is unplugged, the error code information is lost.



This table explains the information for analyzing the cause when an error occurs with the CLD player.

Self-diagnostic error code	Contents	Conditions	Probable cause
H0	Spindle overcurrent detection error.	In the play state, overcurrent was detected in the spindle motor. Monitoring starts 5 seconds after the start of play or special playback mode, this error is detected if the overcurrent port is "L" for 4 seconds.	•Motor NG •Clamper rubbing
U0	FG abnormality error	①At LD start-up, the rate of rotation calculated from the FG was less than 15 rpm for 5 consecutive seconds from the spindle run command. ②At CD start-up, there was less than 1/8th rotation even after 5 seconds had passed since the end of acceleration. ③During play search, CD : subcodes are being read/LD : Phillips codes are being read and the spindle is locked, but a state in which the rate of rotation calculated from the FG was less than 15 rpm continued for 5 seconds or more. In the above case, it is judged that an abnormality has occurred in the FG sensor and that accurate rotation rate calculation has become impossible.	•FG sensor abnormality, FG signal not coming to mechanism controller •FG sensor clogged •Rubbing between FG sensor and slit •Turntable dropped •FG slit deposition NG
H1	Partial short error	①At LD start-up, the speed did not reach 1200 rpm within a certain time (12 seconds) after the spindle run command. ②At CD start-up, a certain speed (313 rpm) was not reached within 6 seconds from the end of spindle acceleration.	•Spindle motor NG •Commutator NG •Bearing too tight •Power supply NG
H2	Power supply abnormality error	– 5V power supply abnormality detected. The power supply abnormality port is constantly monitored and if its signal stays high for about 1 second consecutively, the power supply is judged to be abnormal.	• – 5V not fed from SPDR unit •Parts shorted
L *	Loading error	①When loading operation goes over time (approx. 10 sec.). ②When assist at disc sense entry ends and is not tilt neutral. ③When assist at set up entry ends and is not tilt neutral.	•Tilt switch 1, 2, 3 abnormal, so tilt/loading state not read in correctly •Tilt/loading mechanism mechanically locked •Drive IC NG •Power supply NG

Self-diagnostic error code	Contents	Conditions	Probable cause
E *	Slider error	During slider movement, a time over run occurred (track count search 20 seconds, mandatory movement 10 seconds)	• Slider ceased being able to run • The slider mechanism is mechanically locked and can no longer move to its target. • Slider position switch NG • Flexible cable pulled out • Drive IC NG • Power supply abnormal
U1	Mis clamp error	① During LD setup, after 1/8th rotation, the track count during 1/8 rotation exceeded 511. ② During start-up, the focus was lost once and refocusing was attempted, but the focus could not be locked. ③ When the spindle motor rotation is stopped once before CDV A ⟷ V area change, but stop is not carried out within 2.0 seconds, it is determined that there are two discs on each other and clamp error is set. ④ Two FG pulses did not come within 800 ms from the start of LD start-up. ⑤ During CD start-up, it took more than 860 ms to reach 416 rpm (CD+LD both mounted detected). ⑥ The disc clamp operation did not end within 5 seconds.	• Disc sandwiched • Disc shifted • Spindle motor NG • Disc scratched or dirty defocused during start-up • Two discs loaded • PU actuator NG • Tilt sensor NG • Tilt neutral NG (tilt base NG)
P *	Spindle error	① During TOC reading with an LD, the spindle servo was not locked within 60 seconds from the start of the spindle run. ② When CAV/CLV determination is not finished within 60 seconds from spindle servo lock. ③ The codes could not be read for 10 – 15 seconds consecutively for an LD or 7 – 10 seconds for a CD/CDV and the spindle servo was not locked. ④ The speed exceeded 2100 rpm during LD start-up.	P0: • PH code, SUB-Q code can not be read • VCO, PLL offset out of adjustment • Disc defect P5: • PAL disc, mirror disc, etc. PLAY • No RF P6: • Spindle servo does not lock • Spindle motor NG
F *	Focus error	① "In the "no disc" state, a setup command was received from the mode controller. ② When LD is out of focus when slider is moved to starting position during set up. In case of CD/CDV is NG even after three focus tries. ③ During start-up, the maximum slider servo duty continued for 3 loops or more.	F5: • CD, LD on top of each other • LD scratched or dirty defocused during slider movement • DISC NG • Slider position switch NG F6: • Inner edge of disc scratched or dirty • Slider ran into inner edge mechanical stopper

※ Besides the above errors, there is the "U2" communications error (the mode controller could not communicate normally with the mechanism controller).
※ The probable cause is a defective mechanism controller, disconnected cable, etc..

Mechanism mode contents (meanig of * for L * etc.)

0 : Play	5 : Setup (rotation start)
1 : Open	6 : TOC read
2 : Standby	7 : Play
3 : Clamp	8 : Search
4 : Disc sense	F : Recovery mode

※ 0 : Normal playing
7 : Moving to play operation

6. ADJUSTMENTS

6.1 TEST MODE

1)How to start the test mode

On the MOTHER ASSY, Short circuit the test mode JP W503 and W502, the test mode is started by pressing the power switch ON. (Fig. 1)

After confirming that all FL indicators are lit, remove test mode jumper wire and GND connection. If you have test mode remote control unit (GGF1067), press ESC key and TEST key in order with power switch ON.

2)How to cancel the test mode

Turn power switch OFF. Or, press test mode remote control ESC key.

3)Functions and key control when in test mode

Note : For keys not on player or on accompanying remote control, use test mode remote control unit (GGF1067).

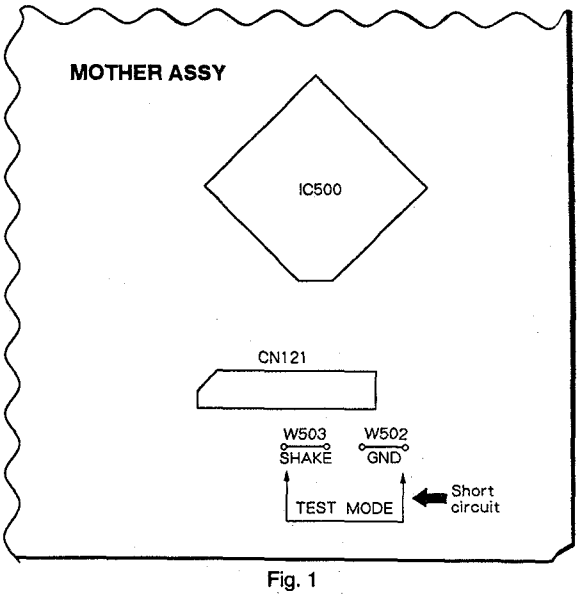


Fig. 1

Note : When you open the tray in test mode, the screen displays goes out. To display the screen again, press the [DISPLAY] key.

- **Key Operation in the Test Mode**

Player Status	Key Operation	Function	TV Screen Display
Tray Open	⏮/⏭ SKIP (Refer to Note 1)	⏮ : Shifts the tray in the closed direction and also raises the turn table while pressing the key. ⏭ : Shifts the tray in the open direction and also lowers the turn table while pressing the key.	
Tray Open	▶ PLAY	Clamps	
Clamp	▶ PLAY	Turns the disc through TRK Servo OFF	TRK-OFF
TRK Servo OFF	▶ PLAY	TRK Servo ON	TRK-ON
TRK Servo ON	▶ PLAY	TRK Servo OFF	TRK-OFF
TILT Neutral	+ MULTI-SPEED	TILT Servo ON	T-□:ON
TILT ON	- MULTI-SPEED	TILT Neutral	T-□:N
TILT Neutral or ON	⏮/⏭ SKIP	Setting TILT Servo to OFF, can force TILT to move.	T-1 to T-E
Clamp	◀◀/▶▶ SCAN	Can force the slider to move	S-LD S-CDV S-CD S-IN
Play	❙❙ PAUSE	Still	
Play	■ STOP	Stop	
Stop	▲ OPEN	Open	
Play	[+10] ⇩ [0] to [9] ⇩ [▶ PLAY]	Set to SEARCH lead address input mode. Designates the SEARCH lead address through keys 0 to 9. Press the CLEAR [C] key if the designated address is incorrect. Searches the designated address upon pressing the PLAY key.	

Note 1 : Press SKIP (⏮/⏭) keys after the tray is set to open state by pressing OPEN (▲) key.
Because, in tray open state, pressing PLAY (▶) key causes it to set to clamp state and SKIP (⏮/⏭) keys can not function properly.

Table 1

• Player Operation in the Test Mode (Disc tray is removed)

Operate the player by selecting a test mode function with the keys on the player or on the remote control unit.

• CD PLAYBACK

① Place the CD disc on the turn table.

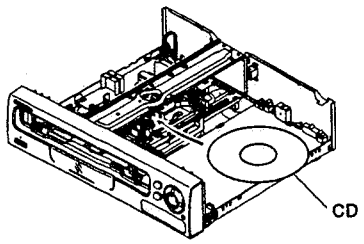


Fig. 2

② Press the PLAY (▶) key once.
(Twin gear starts to move.)

③ Push the cam plate (Fig. 3) in the direction of the arrow and wait until the CD disc is clamped.

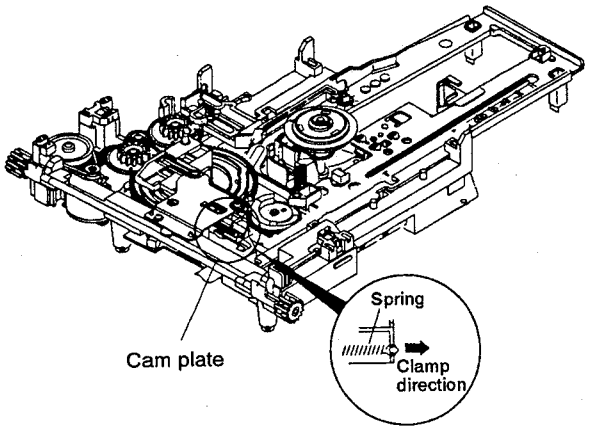
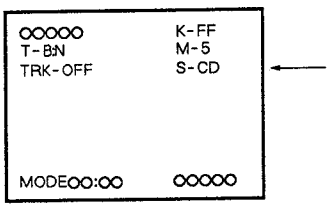


Fig. 3

④ Press the [◀◀] or [▶▶] keys to appear "S - CD" on the TV screen display.



TV screen display

Fig. 4

⑤ After pressing the PLAY (▶) key once to clamp the disc, press the PLAY (▶) key twice, disc will be normally playbacked.

• LD PLAYBACK

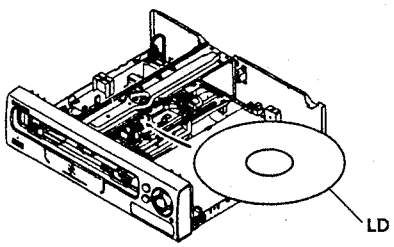


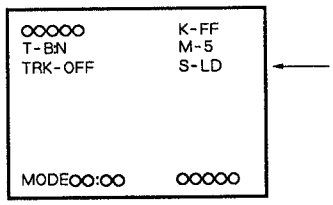
Fig. 5

① press the PLAY (▶) key once.
(Twin gear starts to move.)

② Press the SKIP REV (|◀◀) key to raise the turn table (spindle motor section) while pressing the cam plate (Fig. 3) in the direction of the arrow.
Raise it to the position where the LD disc can be easily placed on the turn table.
If the turn table is raised too high, lower it with the SKIP FWD (▶▶|) key.

③ Place the LD disc on the turn table and press the PLAY (▶) key once to clamp the disc.

④ Press the [◀◀] or [▶▶] keys to appear "S - LD" on the TV screen display.



TV screen display

Fig. 6

⑤ After pressing the PLAY (▶) key once to clamp the disc, press the PLAY (▶) key twice, disc will be normally playbacked.

6.2 ADJUSTMENT PRECAUTIONS

• Equipment and jigs needed for adjustment

- CD test disc (YEDS-7)
- NTSC test disc (GGV1012)
- PAL test disc (GGV1007)
- Medium-sized blade screwdriver
- Small blade screwdriver
- Large Phillips screwdriver
- Medium-sized Phillips screwdriver
- Two-channel oscilloscope (with delay)
- Frequency counter
- TV monitor

• Preparation for Adjustment

1. Disc tray removal

(1) Remove the six screws Ⓐ fastening the bonnet and remove the bonnet.
Remove the two screws Ⓑ holding the PCB holder.

(2) With the power supply on, press the OPEN/CLOSE (LD) button and put the disc tray in the open position.

(3) While pushing the hooks Ⓒ on both sides of the rear of the disc tray inwards, pull out the disc tray.

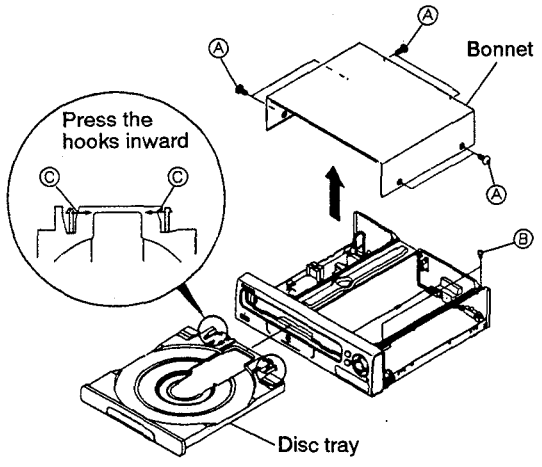


Fig. 7

Note: The adjustments other than "Electrical Adjustments 4. PLL OFFSET Adjustment" can be carried out with the disc tray mounted.

2. Diagnostic method of MOTHER assy

(1) Remove the three screws Ⓓ fastening the rear panel (L). (Fig. 8)

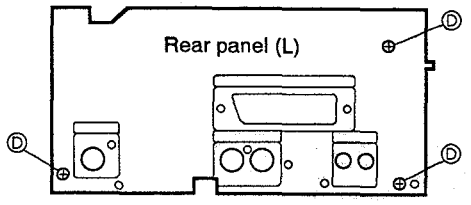


Fig. 8

(2) Remove the two screws Ⓔ fastening the MOTHER assy. (Fig. 9)

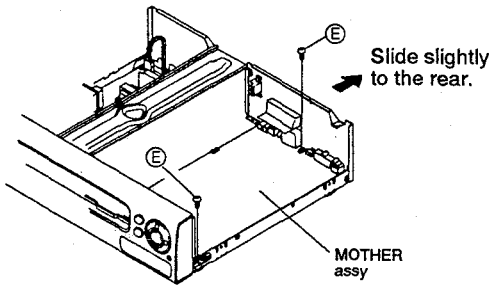


Fig. 9

• The ▶ mark is printed near the Ⓓ and Ⓔ screws.

(3) When you slide the rear panel (L) slightly to the rear, you can remove it together with the MOTHER assy. You can stand it up within the set as in the figure and diagnose the MOTHER assy. (Fig. 10)

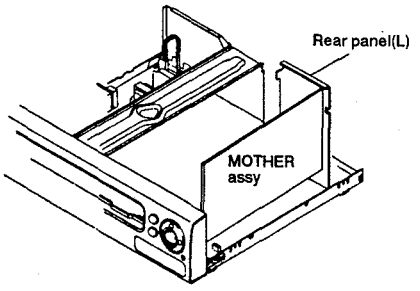


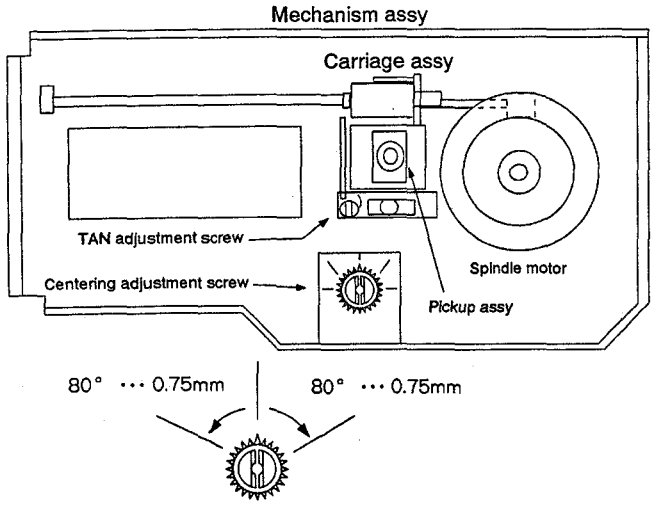
Fig. 10

Note : The MOTHER assy can be diagnosed with the disc tray mounted.

• Before Adjustment Mechanism System

• Centering adjustment screw and TAN adjustment screw

Note : Be careful not to turn centering adjustment screw and TAN adjustment screw past their adjustment range.



Do not turn the Centering and TAN adjustment screws past their ranges, which are ± 0.75mm and ± 80 ° from center.
After the completion of adjustment, apply locktite or the like to the Centering and TAN adjustment screws.
Apply at least 1/3 the circumference about 1/2 half the circumference as in the figure.

Fig. 11 Mechanism assy adjustment

• The mechanical adjustments can all be carried out with disc tray mounted.

• Notes When Adjusting Centering

If waveform S/N is bad and difficult to observe in "3. Spindle motor centering adjustment" use the low pass filter in diagram.

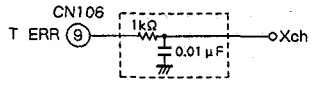


Fig. 12 Low pass filter

• Carriage Assy Position When Adjusting Centering

When moving slider to inner position to adjust the innermost track of disc during centering adjustment, be careful not to keep the mechanism stopper and Carriage assy from bumping each other. (Fig. 13)

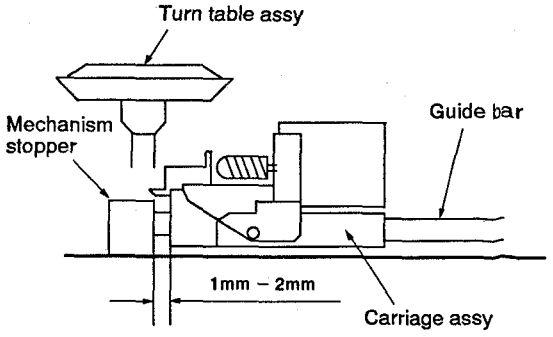


Fig. 13

• Notes When Adjusting Pickup Assy

Please clean lens first when readjusting the PICKUP assy that is on this product. Also, when changing PICKUP assy, change whole CARRIAGE assy (VWT1110).

6.3 ADJUSTMENT LOCATION

VR607: Tilt offset adjustment
VR604: Focus servo loop gain adjustment
VR603: Tracking servo loop gain adjustment
VC502: PAL master clock adjustment (1)
VC503: PAL master clock adjustment (2)
VR450: Output video level adjustment
VR612: PLL OFFSET adjustment
(Order in adjustment)

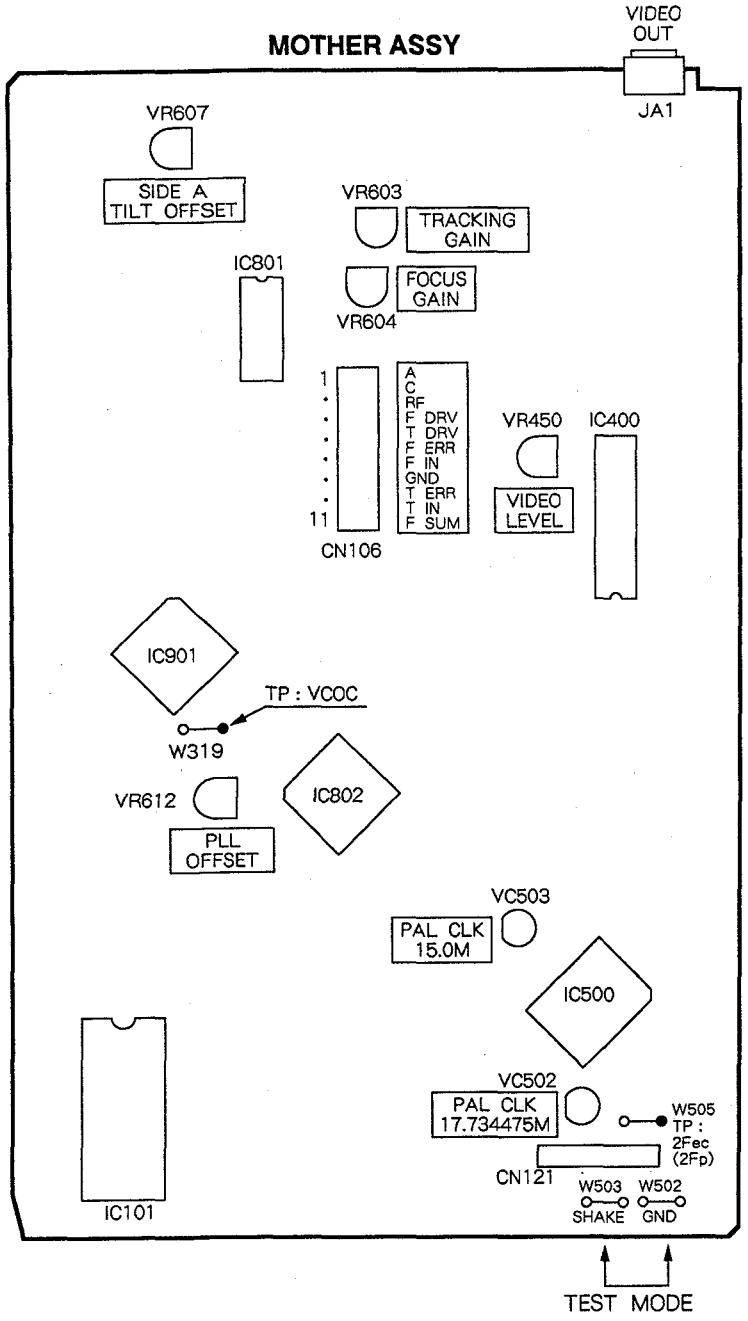
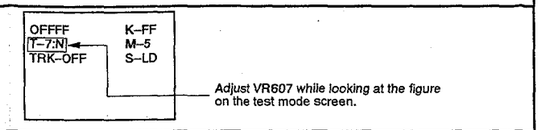
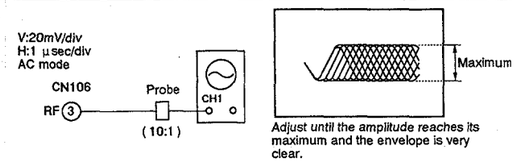
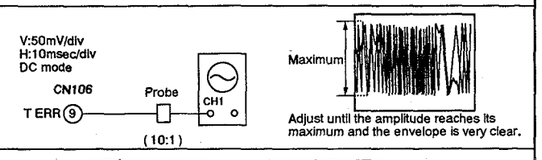
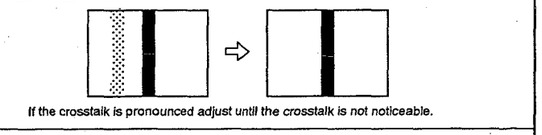
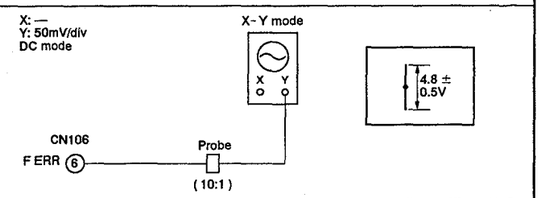
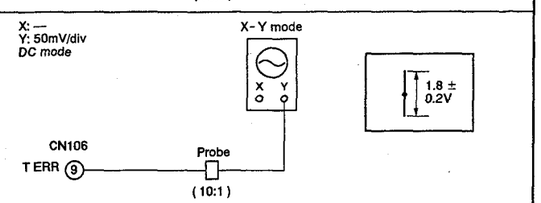
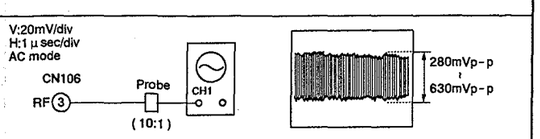


Fig. 14 Adjustment diagram of MOTHER assy

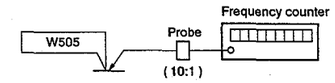
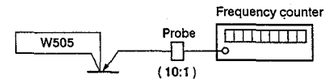
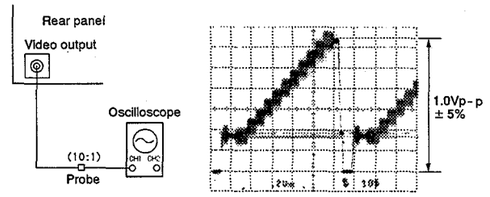
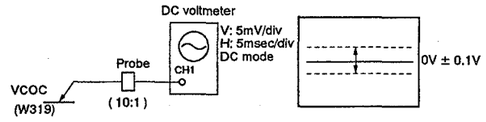
6.4 ADJUSTMENT METHOD

• Mechanical Adustments

Step	Adjustment name	Adjustment point	Measuring point and measuring mode	Player condition	Adjustment procedure	Waveform and connection diagram
1	Tilt offset adjustment	MOTHER assy VR607 (TILT OFFSET)	TV monitor	Test mode Disc not installed	Adjust VR607 so that the tilt indication reaches T-6 to T-8. (See test mode function and key operation)	
2	Tangential direction angle adjustment	Carriage assy TAN adjustment screw	MOTHER assy CN106-3 (RF)	Test mode CD test disc play (CD INSIDE POSITION) TRKG-ON, TILT-ON	Adjust so that the amplitude of the RF waveform reaches its maximum and the envelope is very clear.	
3	Spindle motor centering adjustment	Mechanism assy Centering adjustment screw	MOTHER assy CN106-9 (T ERR)	Test mode CD test disc play (CD INSIDE POSITION) TRKG-OFF, TILT-ON	Adjust so that the amplitude of the tracking error waveform reaches its maximum and the envelope is very clear.	
4	Cross talk check and tilt offset adjustment	MOTHER assy VR607 (TILT OFFSET)	TV monitor Crosstalk monitor check	Test mode NTSC test disc #115 STILL TRKG-ON, TILT-ON	If the crosstalk is pronounced, adjust VR607 until the crosstalk is not noticeable.	
5	Focus servo loop gain adjustment	MOTHER assy VR604 (FOCUS GAIN)	MOTHER assy CN106-6 (F ERR) CH2 "X-Y mode"	Test mode NTSC test disc (PLAY STANDBY) Short CN106-7 (F IN) and 8 (GND), then PLAY (disc not turn)	Adjust VR604 until the waveform level is 4.8 ± 0.5V.	
6	Tracking servo loop gain adjustment	MOTHER assy VR603 (TRKG GAIN)	MOTHER assy CN106-9 (T ERR) CH2 "X-Y mode"	Test mode NTSC test disc #115 STILL TRKG-ON, TILT-ON	Adjust VR603 until the waveform level is 1.8 ± 0.2V.	
7	RF level check	———	MOTHER assy CN106-3 (RF)	Test mode NTSC test disc #115 STILL TRKG-ON, TILT-ON	Check that the RF waveform amplitude is within the range 280mVp-p to 630mVp-p. ※ There is some variation according to the pickup, but it is about 400mVp-p.	

(NOTE)
- This adjustment can be thought to be about the same adjustment as on the manufacturing line with differing adjustment tools. Follow the adjustment procedures even for checking the adjustments.
- When you open the tray in test mode, the screen displays goes out. To display the screen again, press the DISPLAY key.
- The mechanical adjustment can be all carried out with disc tray mounted.

• Electlical Adjustment

Step	Adjustment name	Adjustment point	Measurement point	Player condition	Adjustment procedure	Waveform and connection diagram
1	PAL master clock adjustment (1)	MOTHER assy VC502	MOTHER assy W505 (4fsc)	Normal mode Play the PAL test disc, and next to the stop mode	Adjust VC502 so that the frequency of W505 becomes 17.734475MHz ± 40Hz.	
2	PAL master clock adjustment (2)	MOTHER assy VC503	MOTHER assy W505 (4fp)	Normal mode Play the PAL test disc	Adjust VC503 so that the frequency of W505 becomes 15.0MHz ± 40Hz.	
3	Output video level adjustment	MOTHER assy VR450 (VIDEO LEVEL)	MOTHER assy Video output terminal	Normal mode Play the PAL test disc	Adjust VR450 so that the voltage level of composite video signal between sync tip to 100% white level becomes 1Vp-p ± 5%.	
4	PLL OFFSET adjustment	MOTHER assy VR612 (PLL OFFSET)	MOTHER assy W319 (VCOC)	Test mode TRKG servo OFF Play the CD test disc	1. In the TRKG servo OFF, connect an oscilloscope via low pass filter. 2. Adjust VR612 so that the voltage difference between the PLL OFFSET voltage at FSEQ signal completely down to the GND level and the voltage at normal PLAY state becomes 0V ± 0.1V.	

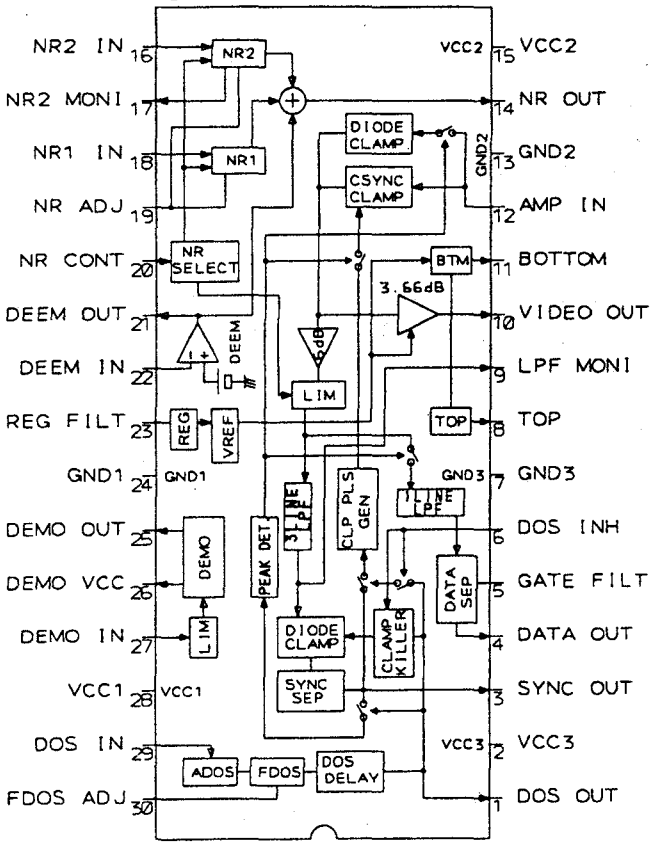
7. IC INFORMATION

- The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

■ PAC005B (MOTHER ASSY : IC400)

• VIDEO IC

• Block Diagram



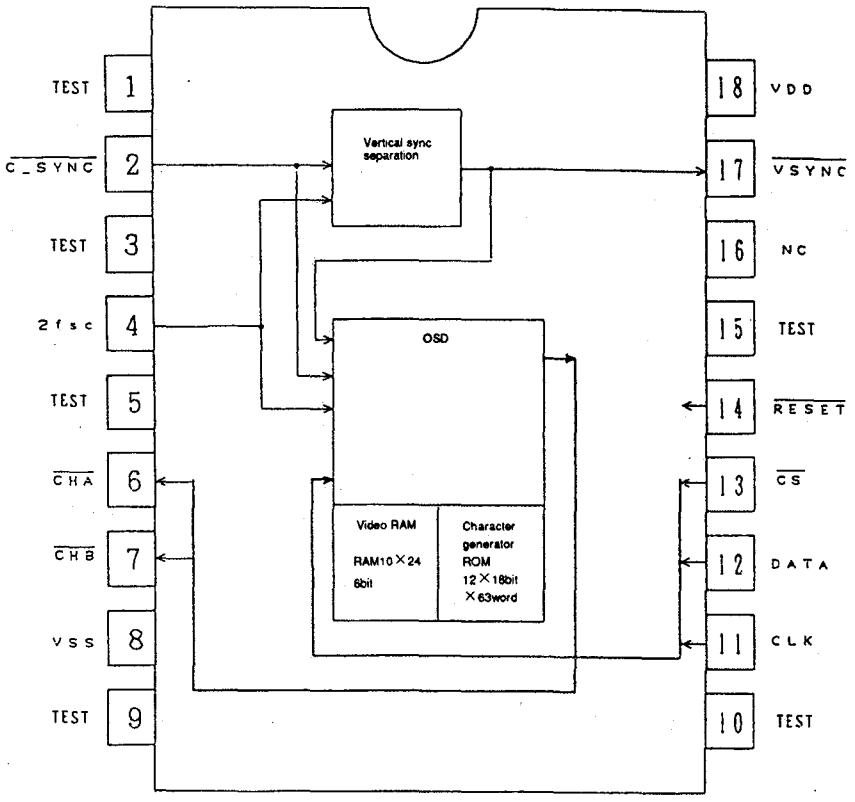
• Pin Function

No.	Pin Name	Function
1	DOS OUT	Drop out pulse output.
2	VCC3	VCC for SYNC SEP section.
3	SYNC OUT	Composite sync output.
4	DATA OUT	Data pulse output.
5	GATE FILT	Connect a capacitor for Date - Gate.
6	DOS INH	Clamp pulse and clamp killer control.
7	GND3	GND for SYNC SEP section.
8	TOP	Reference DC (TOP) for A/D.
9	LPF MONI	Monitor the LPF for SYNC SEP.
10	VIDEO OUT	Signal output for A/D.
11	BOTTOM	Reference DC (BOTTOM) for A/D.
12	AMP IN	Sync chip clamp input.
13	GND2	GND for VIDEO.
14	NR OUT	Noise reduction output.
15	VCC2	VCC for VIDEO section.
16	NR2 IN	Signal input (2) for noise reduction.
17	NR2 MONI	Limitter output for noise reduction.
18	NR1 IN	Signal input (1) for noise reduction.
19	NR ADJ	Limitter level adjusting pin for noise reduction.
20	NR CONT	Noise reduction (1, 2) select and limitter control.
21	DEEM OUT	De-emphasis output.
22	DEEM IN	De-emphasis input.
23	REG FILT	Connect a capacitor for regulator.
24	GND1	GND for RF section.
25	DEMO OUT	Demodulation output of RF signal.
26	DEMO VCC	VCC for FM demodulation output.
27	DEMO IN	RF input for FM demodulation.
28	VCC1	VCC for RF section.
29	DOS IN	RF input for DOS.
30	FDOS ADJ	FDOS sensitivity adjustment.

■ PD9004A (MOTHER ASSY : IC501)

• OSD IC

● Block Diagram



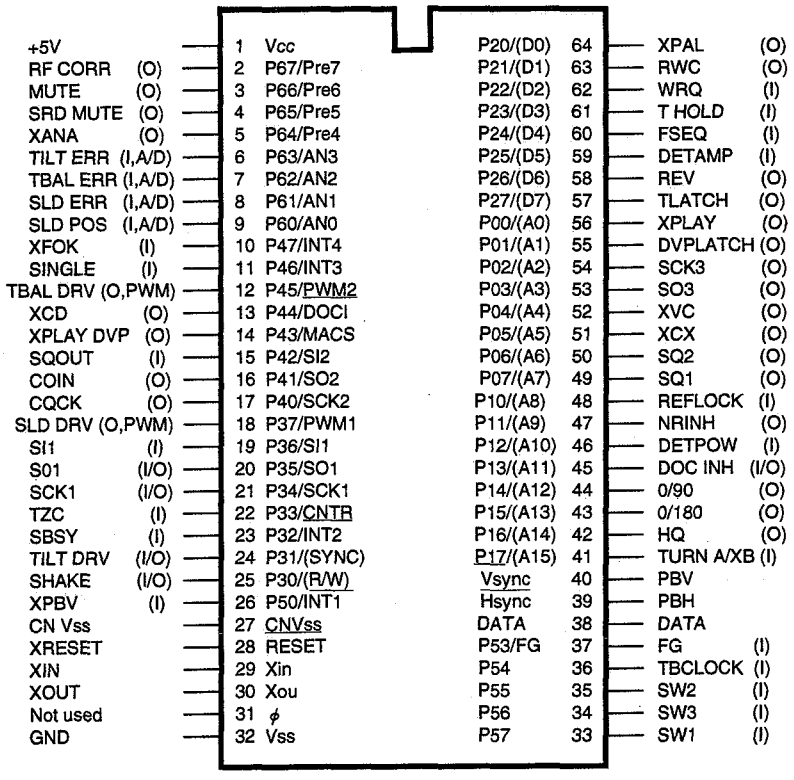
● Pin Function

Pin No	Code	I/O	Logic	Function
1	TEST	—	—	Do not connect any external components.
2	$\overline{\text{CSYNC}}$	I	Negative	Composite sync signal input
3	TEST	—	—	Do not connect any external components.
4	2fsc	I	—	Color subcarrier frequency 2× clock input (NTSC about 7.14 MHz PAL about 8.8 MHz)
5	TEST	—	—	Do not connect any external components.
6	$\overline{\text{CHA}}$	O	Negative	Character timing output
7	$\overline{\text{CHB}}$	O	Negative	Blanking timing output
8	VSS	—	—	Connected to system ground
9	TEST	—	—	Do not connect any external components.
10	TEST	—	—	Do not connect any external components.
11	CLK	I	↑	Data read-in clock input pin; the data applied to the Data pin is read-in at the rising edge of the clock.
12	DATA	I	Positive	Control data input pin; the data is read-in synchronized with the clock applied to the CLK pin.
13	$\overline{\text{CS}}$	I	Negative	Low for serial communications
14	$\overline{\text{RESET}}$	I	Negative	Hardware reset with pull-up resistance
15	TEST	—	—	Do not connect any external components.
16	NC	—	—	Not connected
17	$\overline{\text{VSYNC}}$	O	Negative	Signal with V sync separated from C sync
18	VDD	—	—	Power supply (+5V) pin

■PD0220A (MOTHER ASSY : IC101)

• MECHANISM CONTROL IC

• Pin Assignment (Top view)



• Pin Function

No.	Pin name	I/O	Function
1	Vcc	I	Power supply connection pin. 5V±10% applied.
2	RF CORR	O	RF correction switch signal output pin. "H" =Gain up "H" =Rise up CAV, within #8000 at TOC reading. "L" =others (#8000 - #8100 : hold the previous state.)
3	MUTE	O	Audio system audio mute control signal output pin. "H" =Mute ON, "L" =Mute OFF
4	SRDMUTE	O	AC3 mute control signal output pin. Release mute only during play. "L" =Mute, "H" =Release mute
5	XANA	O	Digital/Analog audio switching signal output pin. "H" =Digital, "L" =Analog
6	TILT ERR	I A/D	Tilt sensor output signal input pin. The tilt motor is controlled to make this signal 2.5V.
7	TBAL ERR	I A/D	Tracking balance error signal input pin(A/D input port). This signal is converted from analog to digital and used for tracking offset control input.
8	SLD ERR	I A/D	Slider error signal input pin (A/D input port). This signal is converted from analog to digital and used for slider servo control input.
9	SLD POS	I A/D	Pickup position detection switch input pin (A/D input port). The switches are resistance divided, the A/D input value read in, and the position detected.
10	XFOK	I	Focus servo lock signal input pin. "L" =lock, "H" =unlock Used for focus servo lock detection.
11	SINGLE	I	Uses the rear panel ATT switch in single mode and communicates this data to the mode controller. "L" =normal, "H" =single
12	TBAL DRV	O PWM	Tracking offset control signal output pin. PWM outputs the tracking offset for use as the auto tracking offset. Period 910 μsec, 3-value control : H, L, Z
13	XCD	O	LD/CD switching signal output pin.
14	XPLAY DVP	O	Spindle servo signal output pin. "L" =during servo, "H" =acceleration, brake, during servo
15	SQOUT	I	DSP reading command data input pin. SUBQ is read out.
16	COIN	O	DSP writing command data output pin.
17	CQCK	O	DSP read/write command clock output pin. Read in at rising edge.
18	SLD DRV	O PWM	Slider control signal output pin. Side A : 5V=FWD, 0V=REV, Side B : 0V=FWD, 5V=REV, 2.5V=STOP, Period 910 μsec, 3-value control : H, L, Z

No.	Pin name	I/O	Function
19	SI1	I	Data input pin from mode controller IC.
20	SO1	O	Serial data output pin to mode controller IC.
21	SCK1	I/O	Clock for serial communication with mode controller IC. Other than when communicating with mode controller IC, input mode.
22	TZC	I	Tracking error zero cross signal input pin. Control the slider motor which is counted this signal in the track count search.
23	SBSY	I	Subcode block sync. signal input pin. "H" =S0, S1, "L" =others
24	TILT DRV	I/O	Load/tilt control output pin. 0.5V - tray in, out/tilt down, up 2.5V - stop Use for tilt servo by PWM output the tilt drive.
25	SHAKE	I/O	Handshake signal pin for data communications with mode controller IC. This pin is a bidirectional data line and control the input/output by the respective microcomputers.
26	XPBV	I	LD/CDV playback vertical sync signal input pin. "L" =during vertical sync.
27	CN Vss	I	Ground for A/D conversion.
28	XRESET	I	Reset signal input pin. "L" =reset, "H" =release reset Controlled by mode controller IC.
29	XIN	I	9MHz clock oscillation input pin.
30	XOUT	O	9MHz clock oscillation output pin.
31	N.C.	O	Dedicated output pin, so other uses prohibited.
32	Vss	I	Ground
33	SW1	I	Switch input pin for loading/tilt position detection.
34	SW3	I	Switch input pin for loading/tilt position detection.
35	SW2	I	Switch input pin for loading/tilt position detection.
36	TBCLOCK	I	Spindle lock signal input pin. "H" =Lock, "L" =Unlock
37	FG	I	Spindle motor FG signal input pin. 16 pulses per rotation, used within microcomputer frequency divided by 2.
38	DATA	I	Mechanism controller built-in Phillips code/decode input pin.
39	XPBH	I	Playback HSYNC input for Phillips coding/decoding.
40	XPBV	I	Playback VSYNC input for Phillips coding/decoding.
41	TURN A/XB	I	Double sided mech. turn switch. "H" =side A , "L" =side B
42	HQON	O	High quality circuit (analog NR) control signal output pin. "H" =through the HQ circuit, "L" =Not through
43	0/180	O	Phase switch signal output pin at PAL trick play. "H" =through the inverter, "L" =through
44	0/90	O	Phase switch signal output pin at PAL trick play. "H" =through the 1H delay line, "L" =through
45	DOC INH	I/O	Control the clamp pulse and clamp killer circuits by 3-value.
46	DETPOW	I	Used as power supply abnormality signal input port. "L" =normal, "H" =abnormal
47	NRINH	O	VDEM noise reduction control output pin. "L" =normal, "H" =no NR
48	REFLOCK	I	Reference signal input pin from DVP. "L" =phase not aligned, "H" =phase aligned
49	SQ1	O	Analog audio switching signal output pin. 1/L squelch : H
50	SQ2	O	Analog audio switching signal output pin. 2/R squelch : H
51	XCX	O	Analog audio CX noise reduction switching signal output pin. "L" =ON , "H" =OFF
52	XVC	O	Voice cancel output. "L" =cancel, "H" =OFF
53	SO3	O	Serial 3 data signal output pin. The serial signals are common and are distinguished with the latch signals (XLAT3, XLAT2 and T LATCH).
54	SCK3	O	Serial 3 clock signal output pin. Reading at rising edge. "H" period : 2 μsec "L" period : 20 μsec
55	DVPLATCH	O	PD6159 serial latch signal output pin. Latches at falling edge.
56	XPLAY	O	In the PAL trick play, video path switching signal output pin at quasi-PAL. "H" =through the PAL special playback circuit. "L" =not through
57	T LATCH	O	Latch signal output pin of serial control for DAC & digital filter IC PD2026A. Latches at falling edge.
58	REV	O	Pickup tension signal output pin at reverse. "H" =side B , "L" =side A
59	DETAMP	I	Spindle overcurrent detection signal input pin. "L" =overcurrent , "H" =normal
60	FSEQ	I	Subcode sync match detection signal input pin. "H" =matches, "L" =does not match
61	T HOLD	I	Track jump accelerating/decelerating signal input pin. "H" =during accelerating/decelerating , "L" =neither
62	WRQ	I	Subcode Q read OK signal input pin. "L" =NG , "H" =This pin goes high when the subcode Q data passes the CRC check.
63	RWC	O	DSP read/write command signal output pin. "L" =read, "H" =write
64	XPAL	O	PAL/NTSC switching signal output pin. "H" =NTSC , "L" =PAL

■ PD6159A (MOTHER ASSY : IC500)

• DUAL DIGITAL VIDEO PROCESSOR IC

• Descriptions

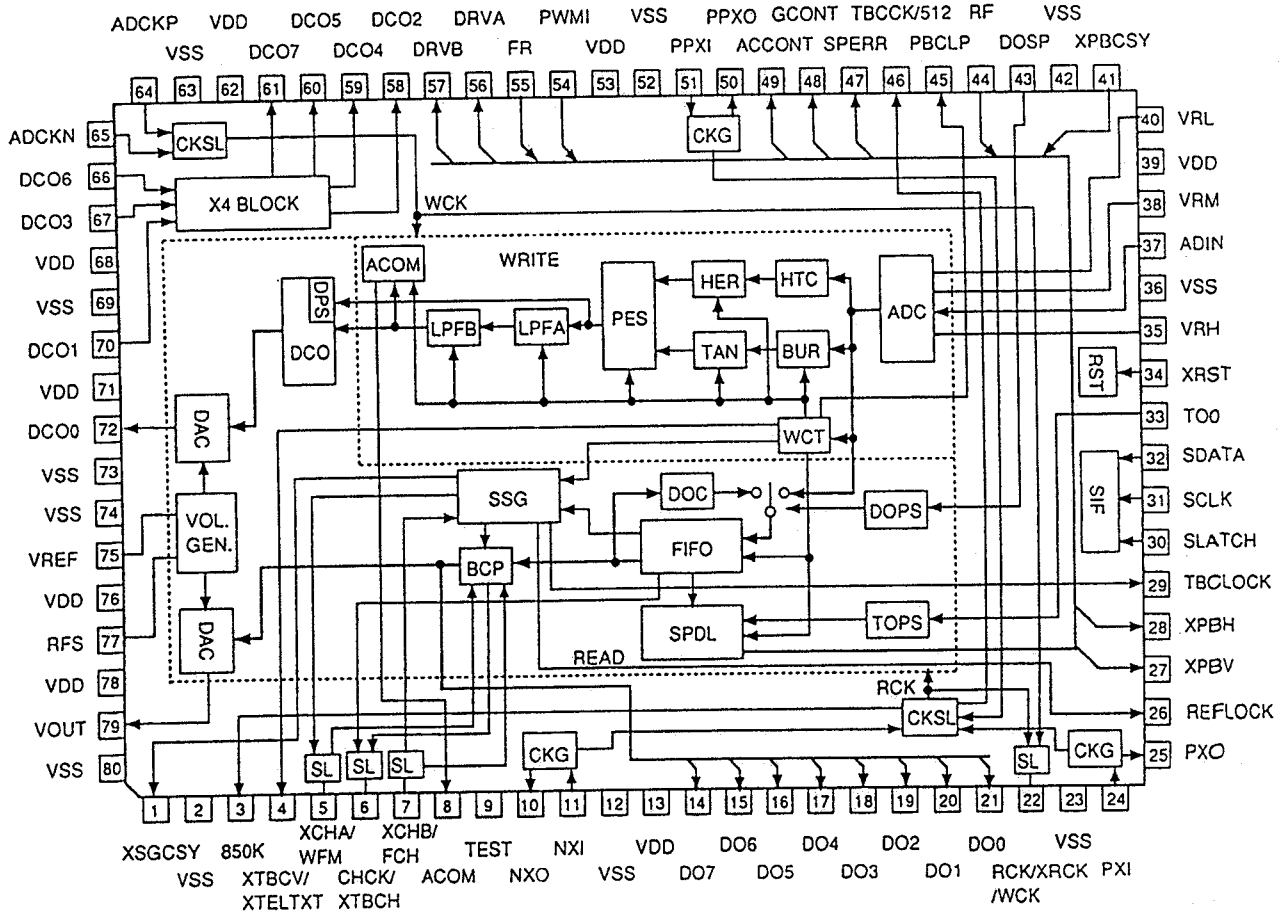
The PD6159A is a digital video processor (DVP) IC designed for dual-CLD players. It supplies time-base-corrected (TBC) video signals (conforming to both PAL and NTSC formats), which have a jitter right after the RF demodulation. It also generates sync signals which synchronize with these output video signals. In addition, various signals required for spindle control are generated by the IC. The PD6159A features the following.

The main functions are compatible with those of the PD0146A (NTSC-exclusive DVP).

Clocks NTSC : 4 fsc
PAL : 4 fp (4x pilot burst for disc video)
4 fsc (for squelch)

Digital TBC
Sync signal generation and synchronization
Generation of a signal for spindle control
Dropout compensation NTSC : Color
PAL : Monochrome
Character-superimpose function
Blue-background generation

• Block Diagram



• Pin Function

No.	Pin Name	I/O	Function	
1	XSGCSY	O	Outputs the reference composite sync from SG with negative logic. While normally in synchronization with the output video signal, it can be specified for free run in memory system mode. (Always synchronized in squelch mode) It can also be delayed by a command with a specified delay duration (SYD0-5).	
2	VSS	–	To be connected to GND. (VSS associated with the logic)	
3	850K	O	Output obtained by exclusive-ORing the NTSC fsc wave with the PAL fsc wave. After passing through an external filter, it can be used as an 850-kHz wave required for NTSC-to-PAL conversion.	
4	XTBCV	O	TELSEL=0	Outputs time-base-corrected V sync with negative logic. In PAL, the timing of the rising can be set to the ends of 23H and 336H by a command (XTBCVSEL).
	XTELTXT	O	TELSEL=1 & NTSC/XPAL=0	Outputs "L" to indicate the teletext data positions (video portion at 20H, 21H, 333H, 334H) in PAL. Fixed to "H" in NTSC.
5	XCHA	I	XCGEN=0	To be connected to the character output of the OSD IC when using the character-superimpose function. When "L" the white level is imposed to the video output.
	WFM	O	XCGEN=1	Outputs "H" for the first field and "L" for the second field.
6	CHCK	O	XCGEN=0	Outputs 2-fsc (2-fp) waves for the OSD IC when using the character-superimpose function. It is synchronized with the RCK/XRCK output.
	XTBCH	O	XCGEN=1	Outputs the time-base-corrected H sync with negative logic.
7	XCHB	I	XCGEN=0	Accepts the character-frame output of the OSD IC when using the character(-frame)-superimpose function. When the input to this pin is "L" and to XCHA is "H" the gray level is imposed on the video output.
	FCH	I	XCGEN=1 & MEMSYS=1	Accepts the field-change signal from the memory controller in memory system mode. "H" at 268H in NTSC or "H" at 315H in PAL during the second field switches the second field to the first field. To be fixed to "L" when not used.
8	ACOM	O	Outputs a signal representing the duty, which depends on the error level obtained at the internal phase comparator. To be used for audio jitter compensation.	
9	TEST	I	To be used when testing the IC. Fix it to "L".	
10	NXO	O	To be connected to the NTSC 4-fsc crystal oscillator.	
11	NXI	I	To be connected to the NTSC 4-fsc crystal oscillator.	
12	VSS	–	To be connected to GND. (VSS associated with the logic)	
13	VDD	–	To be connected to +5 V. (VDD associated with the logic)	
14	DO7	O	To be used normally when OE=1 and OSD0/OSD01=0. A time-base-corrected digital video signal is obtained here in memory mode. DO0 yields the LSB and DO7 the MSB. The signal is in synchronization with the RCK/XRCK output. The squelch data will be output in squelch mode. The data to be output can be selected by commands OSD0/OSD1. When OE=0, these pins are fixed to "L".	
15	DO6			
16	DO5			
17	DO4			
18	DO3			
19	DO2			
20	DO1			
21	DO0			
22	RCK/XRCK	O	OTHERS	Outputs the reference clock (4 fsc for NTSC, 4 fp for PAL video, or 4 fsc for PAL squelch). Positive or negative phase can be selected by a command (RCKSEL).
	WCK	O	OE=1 & OSD=1	Outputs the write clock (4 fsc for NTSC or 4fp for PAL).
23	VSS	–	To be connected to GND. (VSS associated with the logic)	
24	PXI	I	To be connected to the PAL 4-fsc crystal oscillator.	
25	PXO	O	To be connected to the PAL 4-fsc crystal oscillator.	
26	REFLOCK	O	Outputs "H" when the phase difference of H/V sync associated with PB (after TBC) and those associated with SSG is small enough.	
27	XPBV	O	Outputs the signal obtained by separating V sync from the signal at XPBCSY (pin 41) with negative logic.	
28	XPBH	O	Outputs the signal obtained by separating H sync from the signal at XPBCSY (pin 41) with negative logic.	
29	TBCLOCK	O	Outputs "H" when the spindle loop and the TBS loop are locked.	
30	SLATCH	I	Gives the latch timing for data applied to the serial interface. (Through at the rising and no change in register contents during L/H periods and at the falling.)	
31	SCLK	I	Clock inputs for the serial interface. The SDATA value will be read at the rising edge.	
32	SDATA	I	Provides the serial interface with data.	
33	TO0	I	Accepts a tracking-open pulse. The pulse will be internally stretched. The stretch volume is set by a command (STD0 to STD3).	
34	XRST	I	Input for initializing the IC. When "L" all the registers and counters of the IC are set to their initial values.	
35	VRH	I	Provides the AC converter with the reference voltage of the H side.	
36	VSS	–	To be connected to GND. (VSS for the AD converter)	
37	ADIN	I	Input for the AD converter. Accepts a composite video signal having a jitter. In PAL, the pilot burst wave must be in a range of the half the difference between the H reference voltage and the L reference voltage. (See the example of input specifications.)	
38	VRM	I	Intertap pin between the reference resistors. A bypass capacitor can be connected for stabilization.	

No.	Pin Name	I/O	Function
39	VDD	–	To be connected to +5 V. (VDD for the AD converter)
40	VRL	I	Provides the AD converter with the reference voltage for the L side.
41	XPBCSY	I	The PB composite sync is to be supplied here with negative logic.
42	VSS	–	To be connected to GND. (VSS associated with the logic)
43	DOSP	I	Accepts the dropout detection pulse. The pulse will be internally stretched. The stretch volume is set by a command (STD0-3).
44	RF	I	Accepts an RF signal for the spindle servo.
45	PBCLP	O	Flag output to indicate the positions for level clamp of the pilot-burst signal in PAL. (See the example of input specifications.)
46	TBCCK/512	O	Outputs a 1/512th division (approx. 28 kHz) of the clock (NTSC: 4 fsc, PAL: 4 fp) used for TBC. It is used to generate a chopping wave for spindle control.
47	SPERR	O	Output pin for a phase-frequency error of the spindle errors. It outputs the result of comparison between PBH and reference H in tristate. The polarity can be set by a command (PERPOL).
48	GCONT	O	Outputs a PWM signal according to the command-specified value (CD0-3).
49	ACCONT	O	Tristate output of the acceleration/deceleration signal, which depends either on the forced acceleration/deceleration signal, the error detection by RF or error detection by H sync. The acceleration/deceleration volume is determined by setting the duty of the PWM output by commands (RFGD0-3, HFGD0-3). The polarity can be set by a command (ACCPOL).
50	PPXO	O	To be connected to the PAL 4-fp crystal oscillator.
51	PPXI	I	To be connected to the PAL 4-fp crystal oscillator.
52	VSS	–	To be connected to GND. (VSS associated with the logic)
53	VDD	–	To be connected to +5 V. (VDD associated with the logic)
54	PWMI	I	Accepts a signal obtained through the voltage comparison between the spindle error which has passed through a loop filter and the chopping wave externally generated from TBCCK/512.
55	FR	I	Accepts a signal obtained through the voltage comparison between the spindle error which has passed through a loop filter and the destination voltage.
56	DRVA	O	Control signal output for Tr which drives the spindle motor. It is applicable to either a brush motor or brushless motor, selection of which is by a command (BLM). (See the functional block diagram for the logic.)
57	DRVB	O	
58	DCO2	O	Outputs a signal obtained through waveformshaping of the DCO1 signal.
59	DCO4	O	Outputs a signal obtained through waveformshaping of the DCO3 signal.
60	DCO5	O	Outputs a signal multiplied by 2.
61	DCO7	O	Outputs a signal multiplied by 4, which is used as the write clock after passing through a 4-fp or 4-fsc filter.
62	VDD	–	To be connected to +5 V. (VDD for output multiplied by 4).
63	VSS	–	To be connected to GND. (VSS for output multiplied by 4).
64	ADCKP	I	Write clock input for PAL. Accepts the DCO7 output via a 4-fp filter.
65	ADCKN	I	Write clock input for NTSC. Accepts the DCO7 output via a 4-fsc filter.
66	DCO6	I	Accepts a signal obtained by delaying the DCO5 signal by approx. 35 ns.
67	DCO3	I	Accepts a signal obtained by delaying the DCO2 signal by approx. 70 ns.
68	VDD	–	To be connected to +5 V. (VDD for input multiplied by 4).
69	VSS	–	To be connected to GND. (VSS for input multiplied by 4).
70	DCO1	I	Accepts the DCO0 signal via a low-pass filter.
71	VDD	–	To be connected to +5 V. (VDD for the DA converter for DCO0 output).
72	DCO0	O	DC0 output. The signal here is multiplied by 4 to produce ADCK. It can be fixed to the minimum potential by a command (DCOINH).
73	VSS	–	To be connected to GND. (VSS for the DA converter for DCO0 output).
74	VSS	–	To be connected to GND. (VSS for the internal power source for the DA converter).
75	VREF	I	Input to show the reference voltage to the internal power source for the DA converter.
76	VDD	–	To be connected to +5 V. (VDD for the internal power source for the DA converter).
77	RFS	IO	Pin to specify the internal current of the internal power source for the DA converter. Connect 5.1 kohms as standard between this pin and GND.
78	VDD	–	To be connected to +5 V. (VDD for the DA converter for VOUT output).
79	VOUT	O	Time-base-corrected video output. While a composite sync is normally inserted, the sync position will be found at the pedestal level in memory system mode. (However, some half-H pulses etc. may partly remain near V sync.)
80	VSS	–	To be connected to GND. (VSS for the DA converter for VOUT output)

■PD3313A (FLKY ASSY : IC101)

• MODE CONTROL IC

• Pin Function

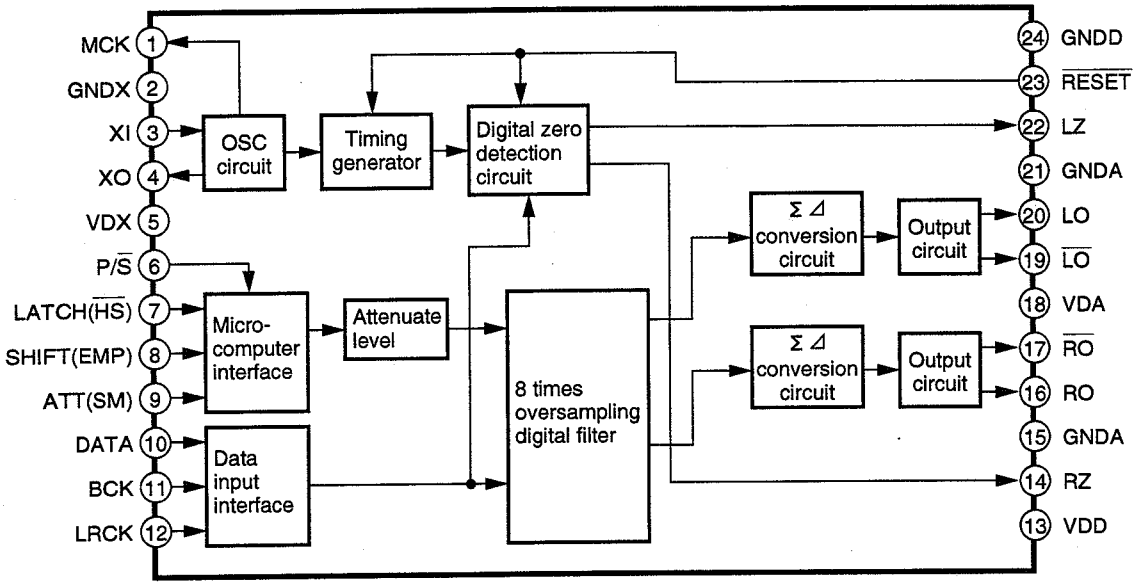
Note : H : HIGH level , L : LOW level , — : High impedance, P : Pulse

No.	Pin name	I/O	Function	No.	Pin name	I/O	Function
1	Vcc	—	+5V power supply.	33	XMIC ON	O	Mic circuit output mute cancel. (L : enable)
2	XRESET	O	MOTHER ASSY reset output.	34	n	O	Display segment output.
3	XSCK	I/O	Serial communication clock. (mechanism control and character generator)	35	KS4/m	O	Key scan output/Display segment output.
4	S MTOF	I	Serial communication data input. (mechanism control)	36	KS3/l	O	Key scan output/Display segment output.
5	S FTOM	O	Serial communication data output. (mechanism control and character generator)	37	KS2/k		
6	XCS	O	Character generator (PD9004A) chip select output. (L : enable)	38	KS1/j		
7	NC	O	Not used.	39	KS0/i		
8	SECAM	I	Trident TV correspondence. H:correspondend, L:not correspondend	40	h	O	Display segment output.
9	POWER ON	O	Power supply switching output of the MOTHER ASSY.	41	g		
10	AVcc	—	+5V power supply.	42	f		
11	KIN0	I	Key data input.	43	e		
12	KIN1			44	d		
13	KIN2			45	c		
14	KIN3			46	b		
15	KIN4			47	a		
16	SW1	I	H : PAL model, L : DUAL model	48	Vdisp	—	Power supply for VFD (-29V) .
17	SW2	I	PAL AFM H : present, L : absent	49	G8	O	Display grid output.
18	SW3	I	PAL trick play H : present, L : absent	50	G7		
19	AVss	—	GND.	51	G6		
20	TEST	I	Connect to GND. (not used)	52	G5		
21	X1	I	NC (not used)	53	G4		
22	X2	I	Connect to +5V. (not used)	54	G3		
23	Vss	—	GND	55	G2		
24	OSC1	I	System clock oscillator connection pin.	56	G1		
25	OSC2	O		57	LED_LD	O	LD tray open/close LED output.
26	XRESET	I	CPU reset (L : reset)	58	LED_CD	O	CD tray open/close LED output.
27	SHAKE	I/O	Mechanism control serial communication requirement.	59	STDBY	O	Standby LED output.
28	SEL IR	I	Remote control input.	60	NC	O	NC
29	FSX	I	7.35MHz frame sync. signal of EFM decoder.	61	NC	O	NC
30	EFLG	I	Error correction state signal of EFM decoder.	62	NC	O	NC
31	GND	—	Ground	63	NC	O	NC
32	WDF	O	For WATCHDOG pulse output.	64	NC	O	NC

■TC9400F (MOTHER ASSY:IC201)

• D/A CONVERTER

• Block Diagram



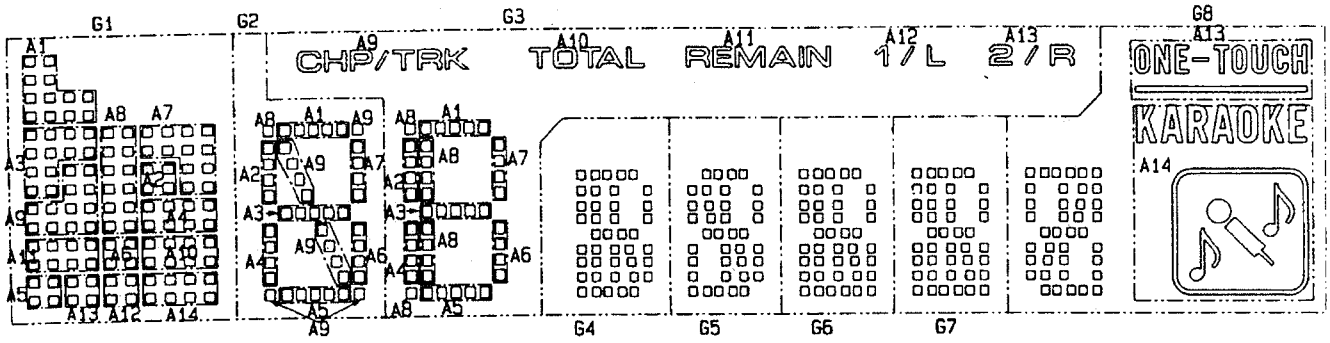
• Pin Function

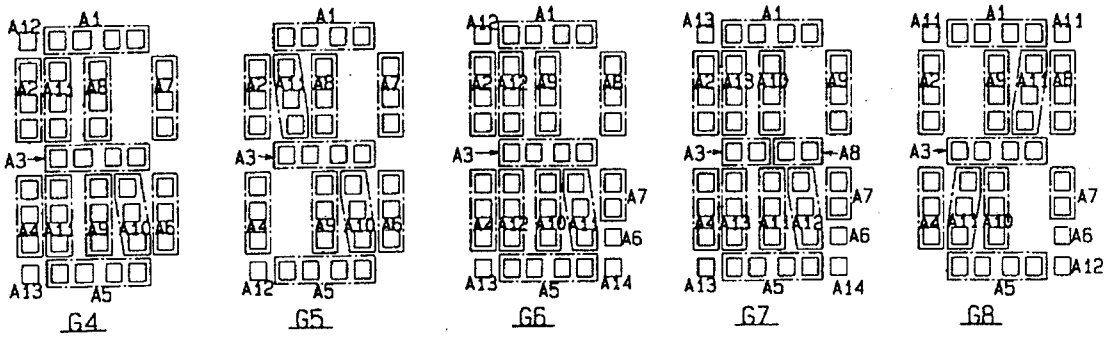
No.	Pin name	I/O	Function
1	MCK	O	System clock supply pin.
2	GNDX	—	Ground pin of oscillation section.
3	XI	I	Crystal oscillator connection pin. Generates a clock for system.
4	XO	O	
5	VDX	—	Power supply pin for oscillation section.
6	P/S	I	Parallel/serial control switching pin. (Schmitt input and pull-up resistor)
7	LATCH (HS)	I	In the serial control, data latch signal input pin for attenuator. In the parallel control, normal/double speed mode selection pin. (Schmitt input and pull-up resistor)
8	SHIFT (EMP)	I	In the serial control, shift clock input pin for attenuator. In the parallel control, deemphasis filter ON/OFF control pin. (Schmitt input and pull-up resistor)
9	ATT (SM)	I	In the serial control, data I input pin for attenuator. In the parallel control, soft mute control pin. (Schmitt input and pull-up resistor)
10	DATA	I	Data input pin. (Schmitt input)
11	BCK	I	Bit clock input pin. (Schmitt input)
12	LRCK	I	LR clock input pin. (Schmitt input)
13	VDD	—	Power supply pin for digital section.
14	RZ	O	R-ch digital zero detection output pin.
15	GNDA	—	Ground pin for R-ch analog section.
16	RO	O	R-ch data positive-phase output pin.
17	RO	O	R-ch data negative-phase output pin.
18	VDA	—	Power supply pin for analog section.
19	LO	O	L-ch data negative-phase output pin.
20	LO	O	L-ch data positive-phase output pin.
21	GNDA	—	Ground pin for L-ch analog section.
22	LZ	O	L-ch digital zero detection output pin.

8. FL INFORMATION

■ VAW1035 (FLKY ASSY : V101)

FL TUBE





ANODE GRID ASSIGNMENT & PIN ASSIGNMENT

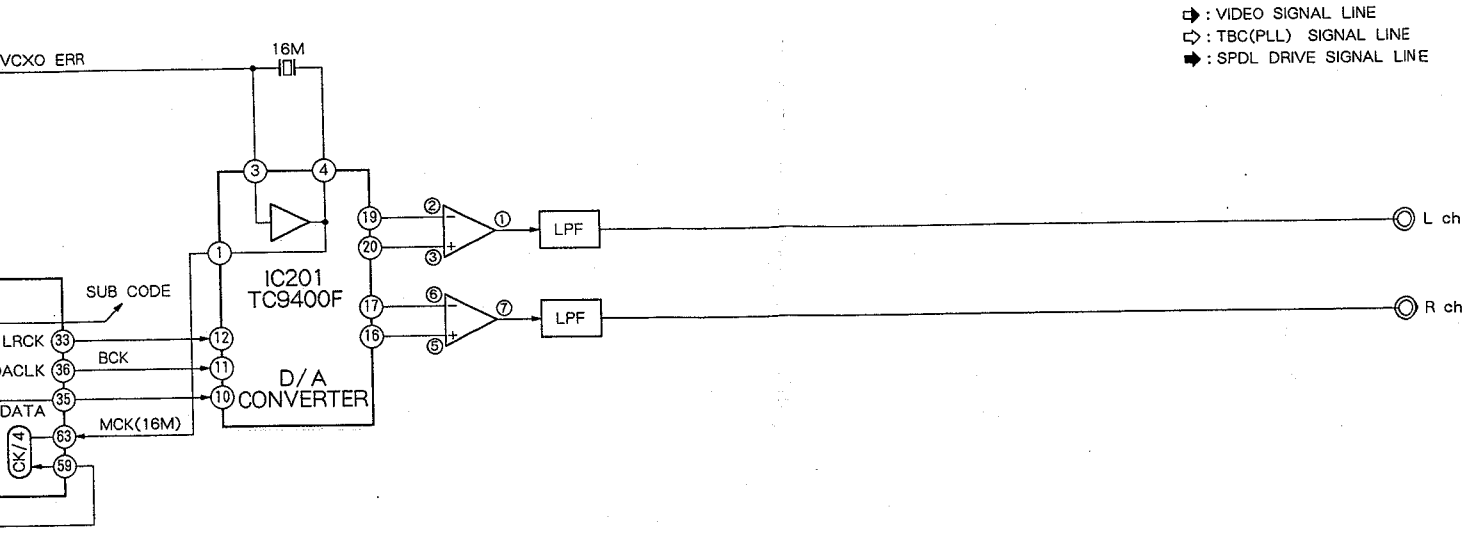
	G1	G2	G3	G4	G5	G6	G7	G8
P1	A1	A1	A1	A1	A1	A1	A1	A1
P2	A2	A2	A2	A2	A2	A2	A2	A2
P3	A3	A3	A3	A3	A3	A3	A3	A3
P4	A4	A4	A4	A4	A4	A4	A4	A4
P5	A5	A5	A5	A5	A5	A5	A5	A5
P6	A6	A6	A6	A6	A6	A6	A6	A6
P7	A7	A7	A7	A7	A7	A7	A7	A7
P8	A8	A8	A8	A8	A8	A8	A8	A8
P9	A9	A9	CHP/TRK	A9	A9	A9	A9	A9
P10	A10		TOTAL	A10	A10	A10	A10	A10
P11	A11		REMAIN	A11	A11	A11	A11	A11
P12	A12		1/L	A12	A12	A12	A12	A12
P13	A13		2/R	A13		A13	A13	ONE-TOUCH
P14	A14					A14	A14	KARAOKE

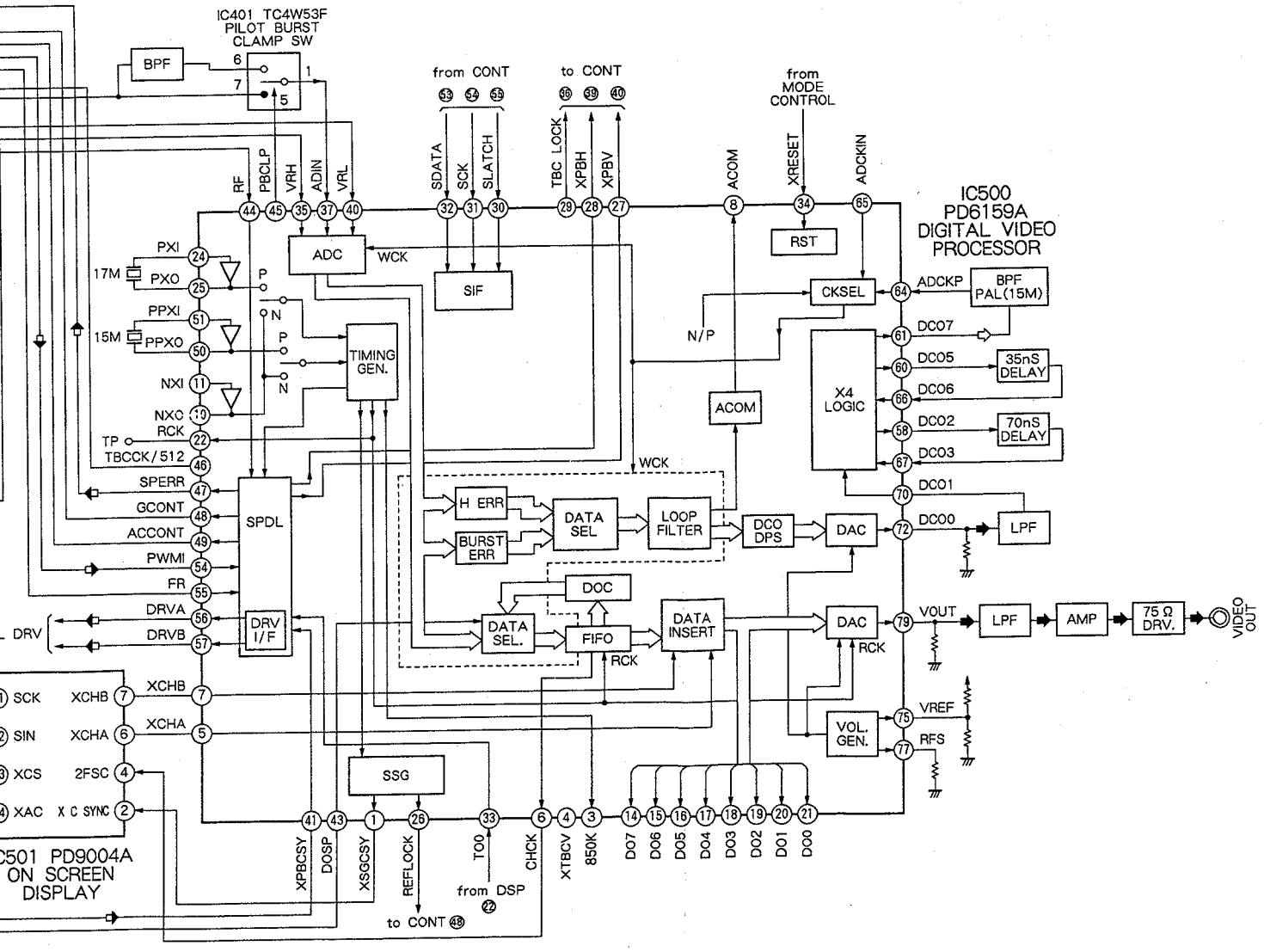
PIN ASSIGNMENT

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Assignment	F	F	NP	NL	NL	NL	NL	G1	G2	G3	G4	G5	G6	G7	G8	P1	P2

Pin No.	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
Assignment	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	NL	NL	NP	F	F

F:Filament G1~G8:Grid P1~P14:Anode NP:No pin NL:No Lead


: VIDEO SIGNAL LINE
: TBC(PLL) SIGNAL LINE
: SPDL DRIVE SIGNAL LINE
VCXO ERR
16M
IC201
TC9400F
D/A
CONVERTER
LPF
LPF
L ch
R ch
SUB CODE
LRCK
BCK
DATA
MCK(16M)
CK/4


IC401 TC4W53F
PILOT BURST
CLAMP SW
BPF
from CONT
to CONT
from
MODE
CONTROL
SDATA
SCK
SLATCH
TBC LOCK
XPBH
XPBV
ACOM
XRESET
ADCKIN
RF
PBCLP
VRH
ADIN
VRL
IC500
PD6159A
DIGITAL VIDEO
PROCESSOR
RST
ADC
WCK
SIF
CKSEL
ADCKP
BPF
PAL(15M)
PXI
17M
PXO
PPXI
15M
PPXO
NXI
NXO
RCK
TP
TBCCK/512
TIMING
GEN.
N/P
X4
LOGIC
DCO7
DCO5
35nS
DELAY
DCO6
DCO2
70nS
DELAY
DCO3
DCO1
DCO0
SPERR
GCONT
ACCONT
PWMI
FR
DRVA
DRVB
SPDL
DRV
I/F
H ERR
BURST
ERR
DATA
SEL
LOOP
FILTER
DCO
DPS
DAC
LPF
DOC
DATA
SEL.
FIFO
DATA
INSERT
DAC
VOUT
LPF
AMP
75 Ω
DRV.
VIDEO
OUT
RCK
VOL.
GEN.
VREF
RFS
SCK
SIN
XCS
XAC
XCHB
XCHA
2FSC
X C SYNC
SSG
C501 PD9004A
ON SCREEN
DISPLAY
XPBCSY
DOSP
XSGCSY
REFLOCK
TOO
CHCK
XTBCV
850K
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DO0
from DSP
to CONT

11. SPECIFICATIONS

1. General

System ..... LaserVision Disc system and Compact Disc digital audio system
Laser ..... Semiconductor laser wavelength 780 nm
Power requirements ..... AC 220 ~ 240 V, 50/60 Hz
Power consumption ..... 25 W
Weight ..... 5.7 kg
Dimensions ..... 420 (W) x 381 (D) x 120 (H) mm
Operating temperature ..... +5°C ~ +35°C
Operating humidity ..... 5% ~ 85%
(There should be no condensation of moisture.)

2. Video characteristics

Format ..... PAL specifications
Video output
Level ..... 1 Vp-p nominal, sync. negative, terminated
Impedance ..... 75Ω unbalanced
Jack ..... RCA jack

3. Audio characteristics

Output level
During digital audio output ..... 200 mVrms (1 kHz, -20 dB)
Jacks ..... Both RCA jacks
Number of channels 2

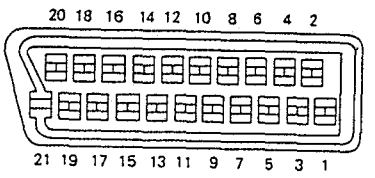
Digital Audio Characteristics

Frequency response	4 Hz - 20 kHz
SN ratio	98 dB (EIAJ)
Dynamic range	94 dB (EIAJ)
Total harmonic distortion	0.005 % (EIAJ)
Wow and flutter	Limit of measurement (EIAJ)

4. Other Terminals

Control input/output ..... Both miniature jacks
AV connector output ..... 21-pin connector
This connector provides the video and audio signals for connection to a colour video TV monitor (or TV set) which has a "AV CONNECTOR" terminal.

PIN assignment



PIN no.		
1	Audio 2/R out	17 GND
3	Audio 1/L out	19 Video out
4	GND	21 GND
8	Status	

5. Accessories

Remote control unit 1
Size "AA" (IEC R6P) dry cell batteries 2
Operating instructions 1
Warranty card 1

NOTE:

The specifications and design of this product are subject to change without notice, due to improvements.